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MS-7883

Haswell-E Platform

ATX

Ver: 11

CPU:

Haswell-E

System Chipset:

Wellsburg

Onboard Chip:

HD Audio Codec: ALC1150

LAN-Killer LAN

LAN-Killer LAN

SIO:NTC6792D

Dual Flash ROM: SPI 64 MB X2

Main Memory:

DDRIV (1666MHz) * 8 (Dual Channel)

ACPI:

ISL6388

PWM:

VRD12.5 -ISL6388

Expansion Slots:

PCI Express (X16) Slot1

PCI Express (X8) Slot2

PCI Express (X16) Slot3

PCI Express (X16) Slot4

PCI Express (X8) Slot5

Other:

SATA3.0 *8


USB2.0 *8

USB3.1 *1

REAL USB3.0 *6

FRONT USB2.0 *4

FRONT USB3.0 *4



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MS-7883

Size Custom

Document Description

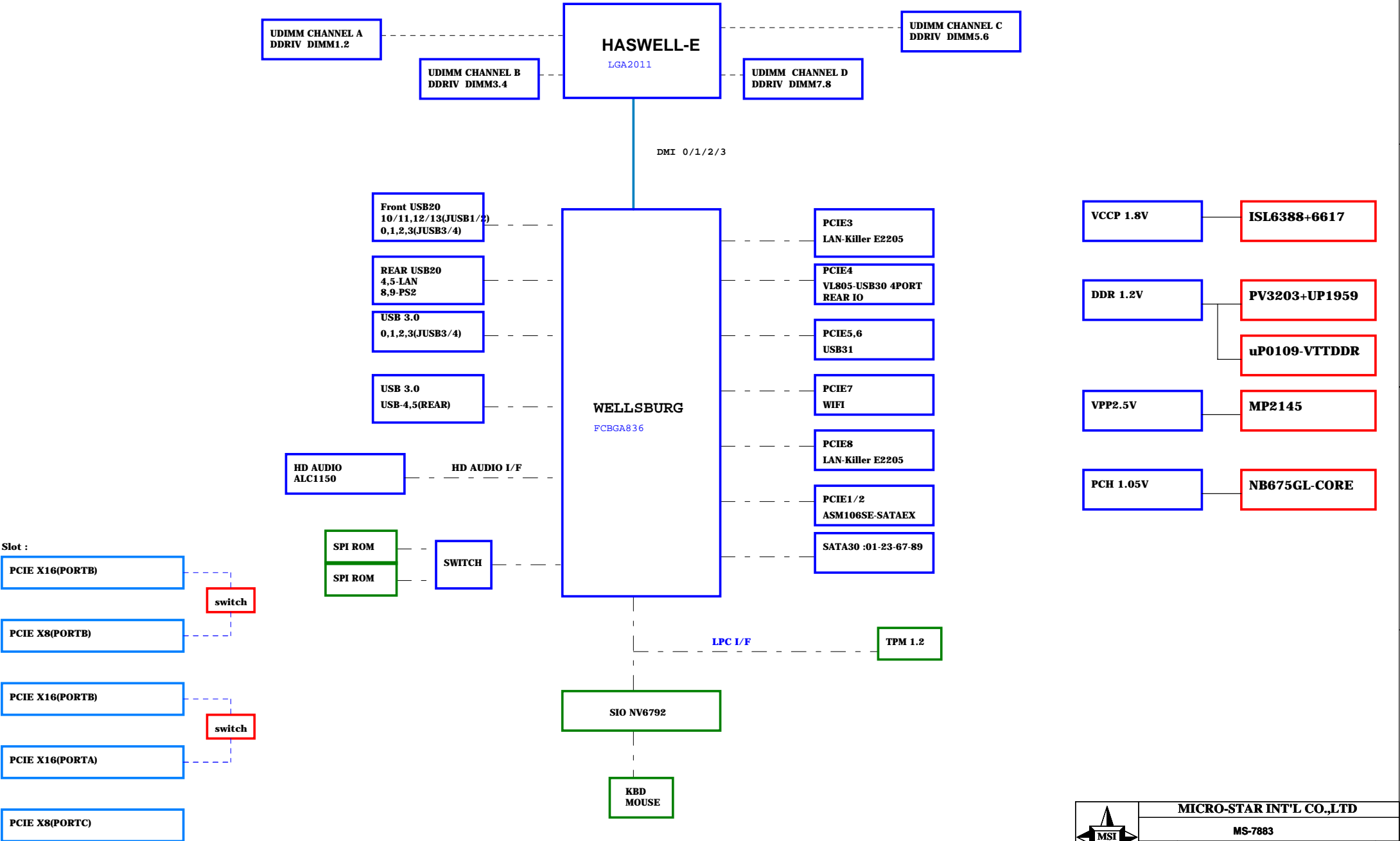
Rev 1.1

Date: Thursday, June 04, 2015

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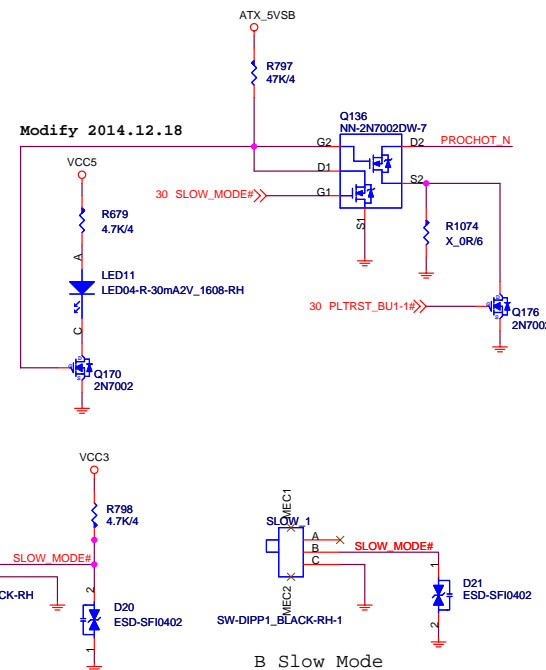
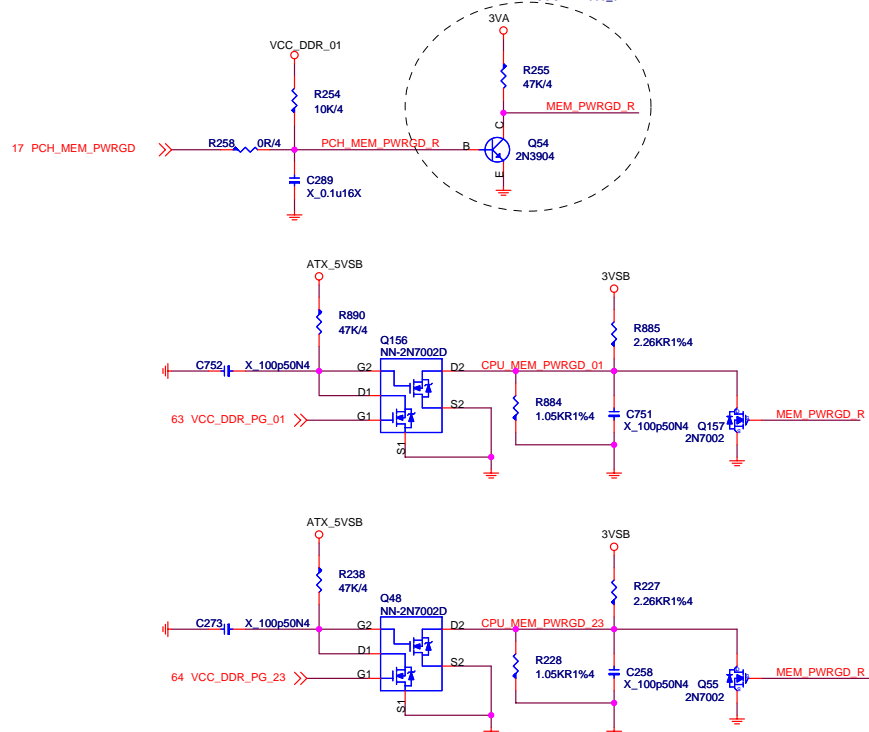
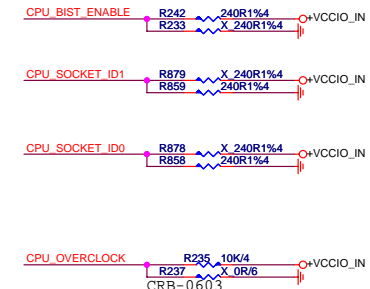
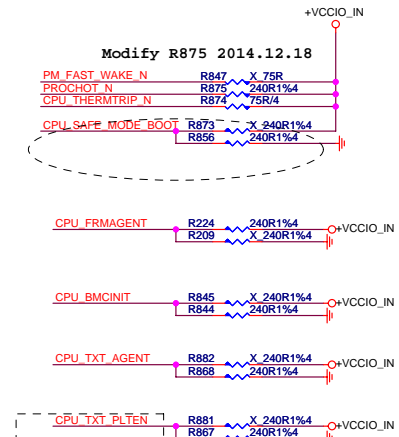
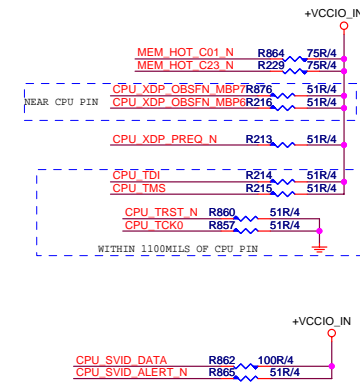
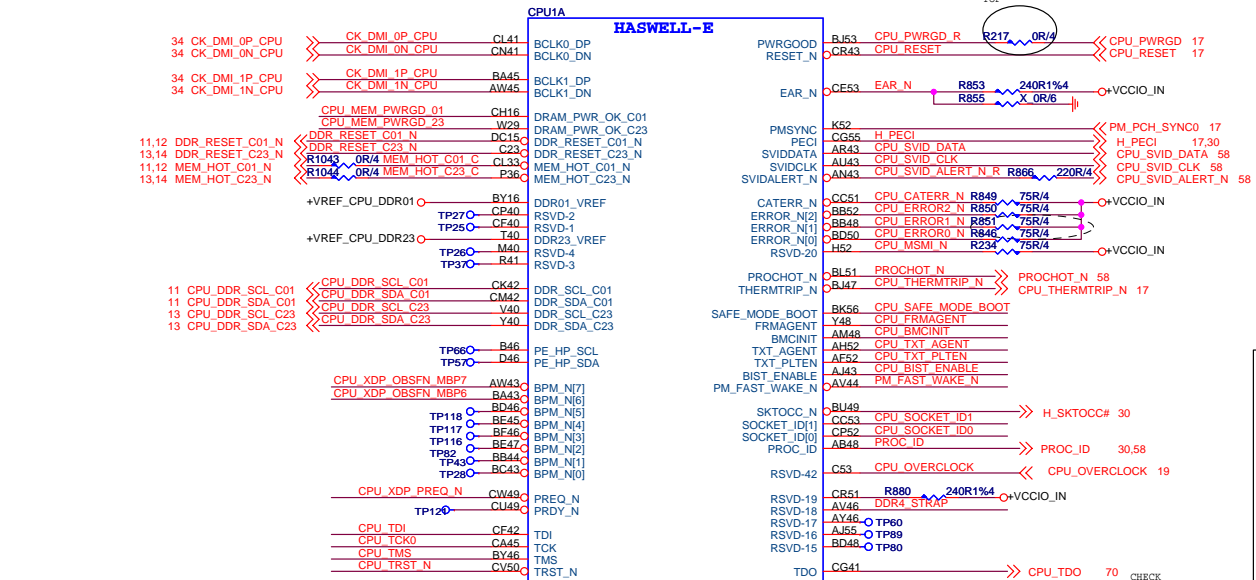
Cover Sheet

MS-7882 Block Diagram



CPU-CLK/Control/MISC

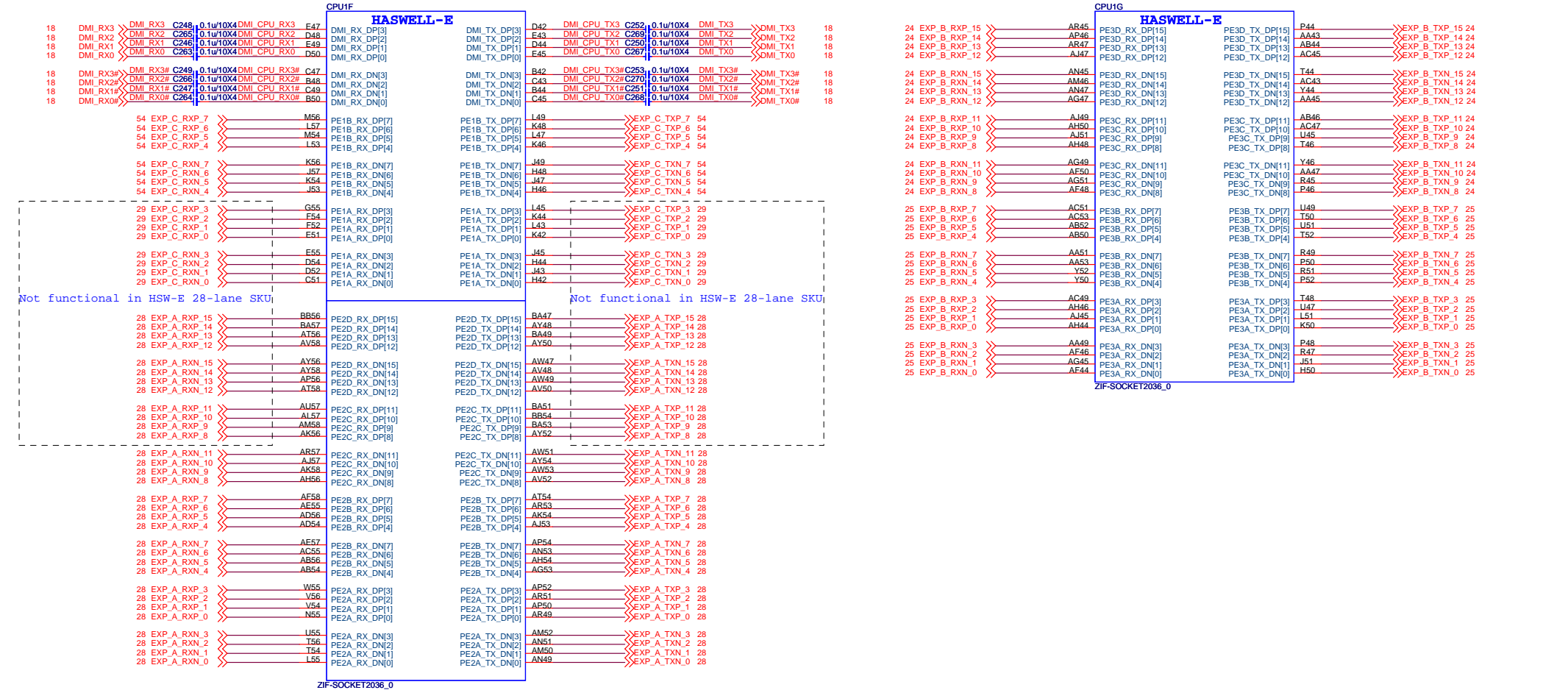
OR:R278 REMOVED

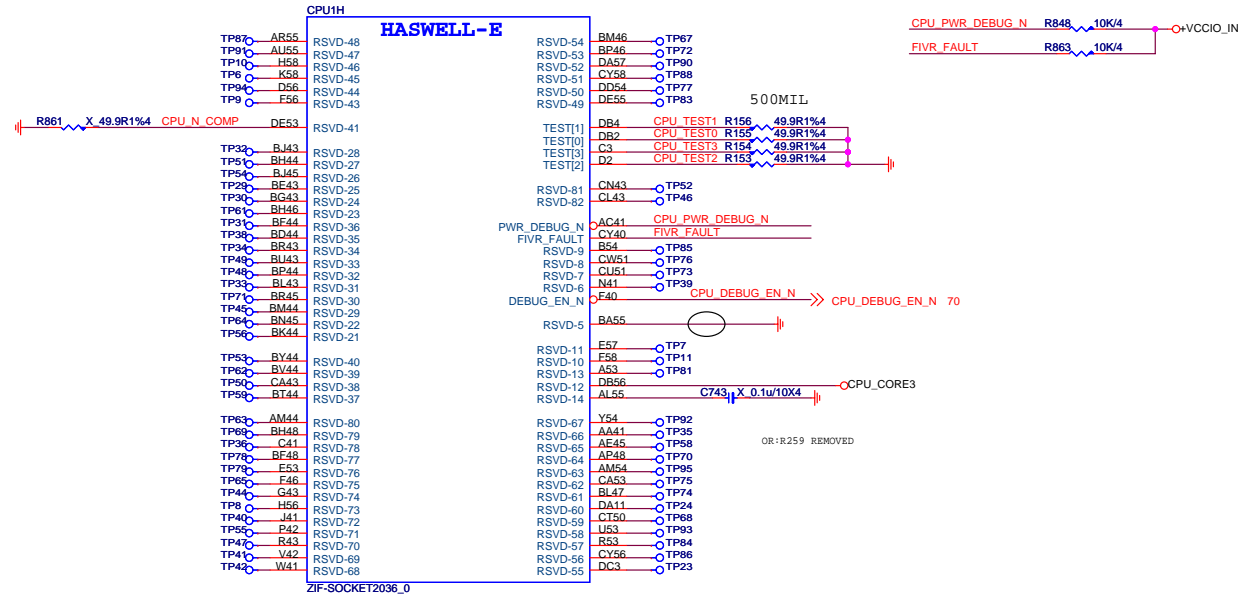
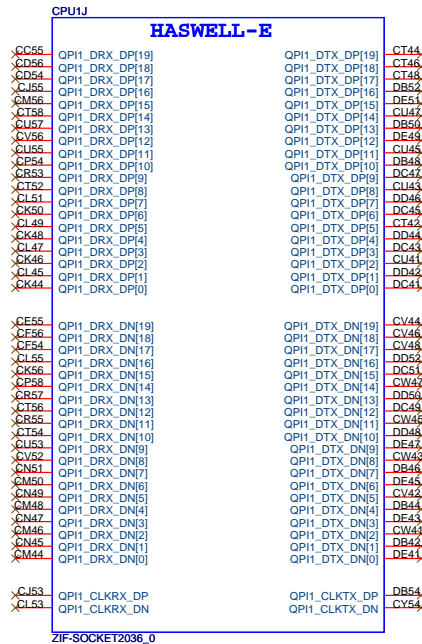
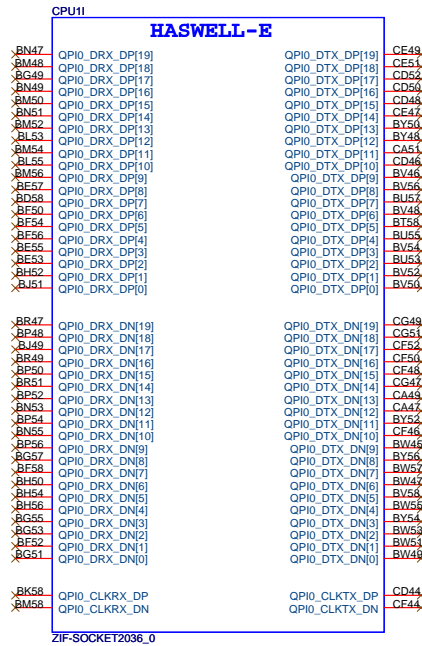


PROC_ID	+VCCIO_IN
0	0.95V
1	1.05V



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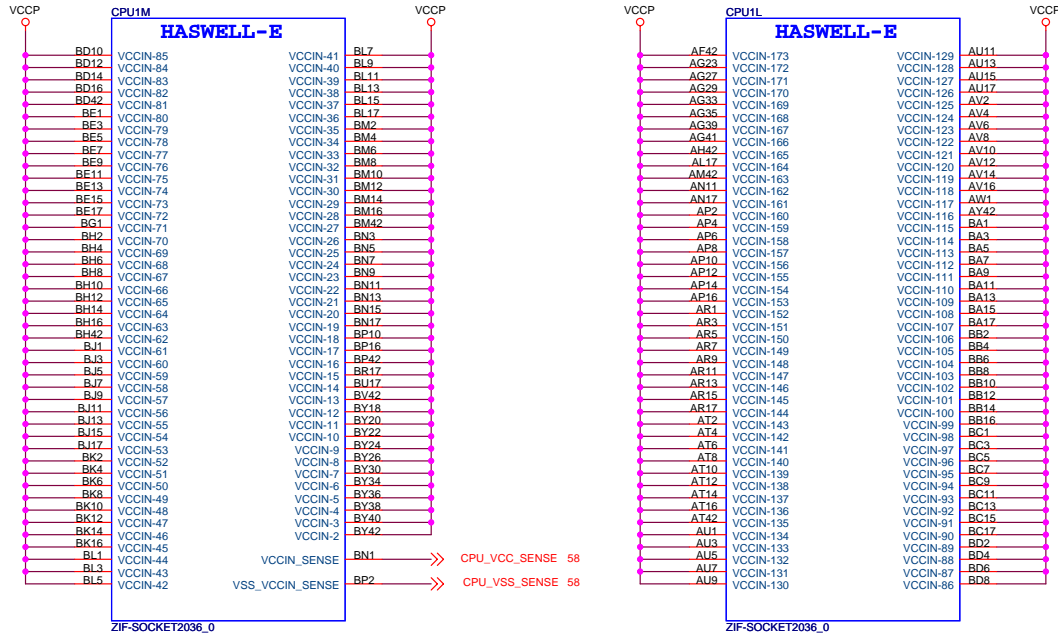
MICRO-STAR INT'L CO.,LTD

MS-7883

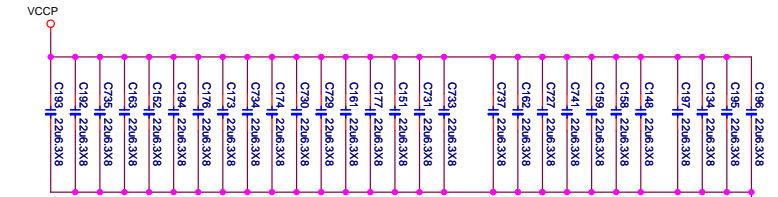
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Custom	CPU-QPI/RESERVE	1.1

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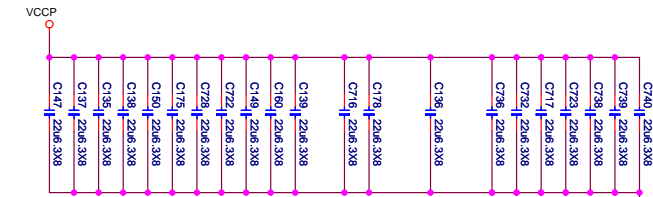
CPU-Power



+CPU_VCCP-Decoupling



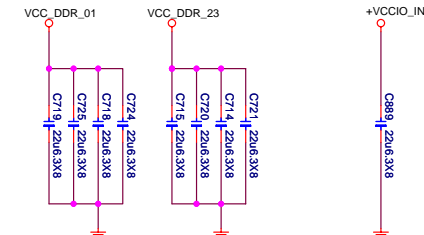
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY



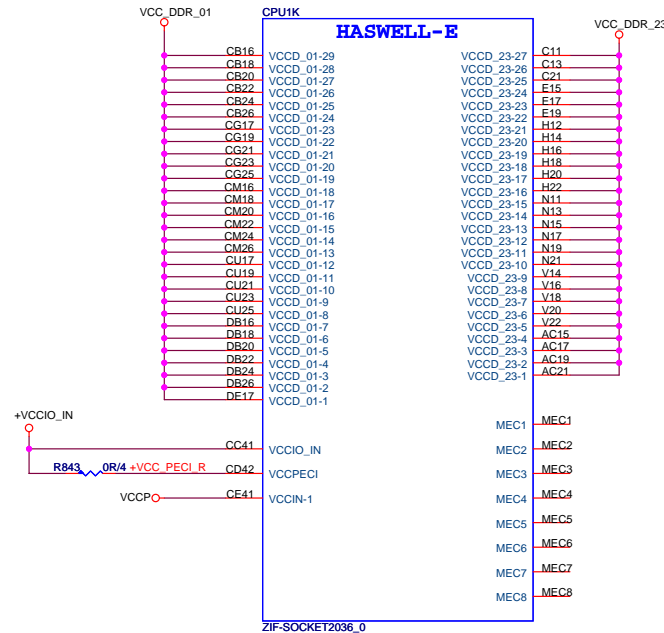
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

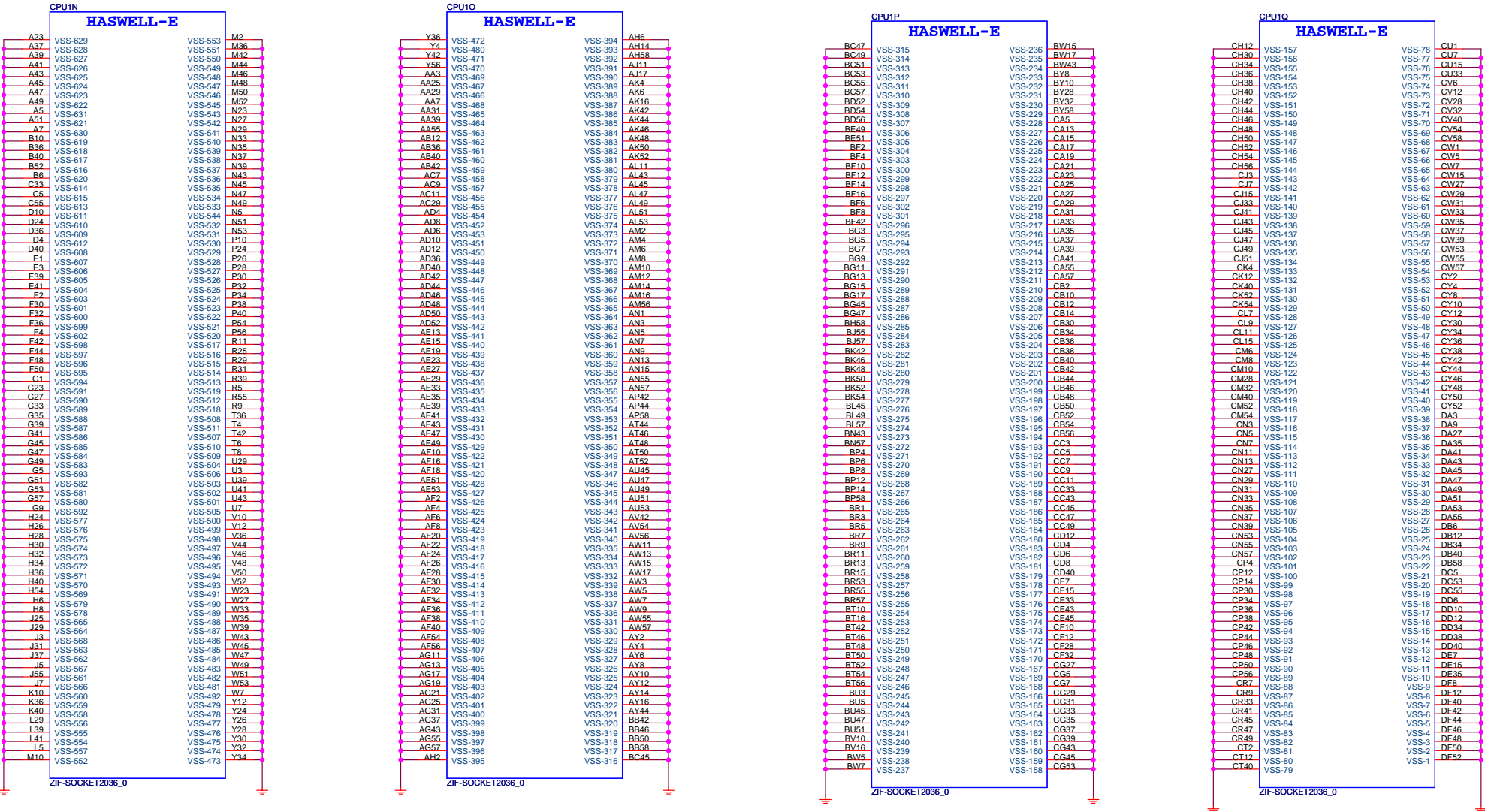
Skt cavity caps, place: 28 on top side & 26 on back side.

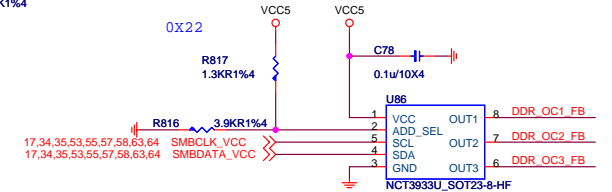
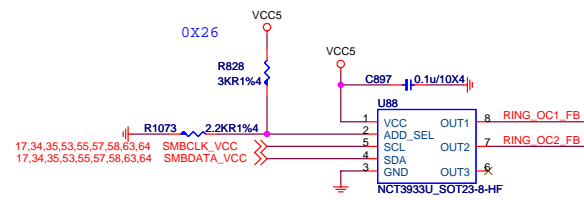
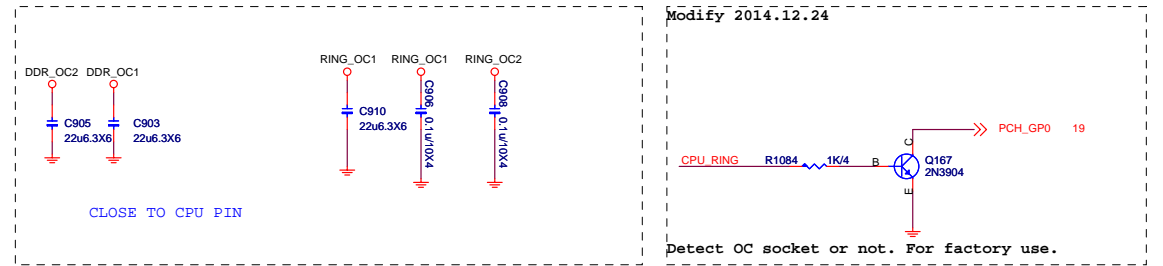
+CPU_DDR-Decoupling



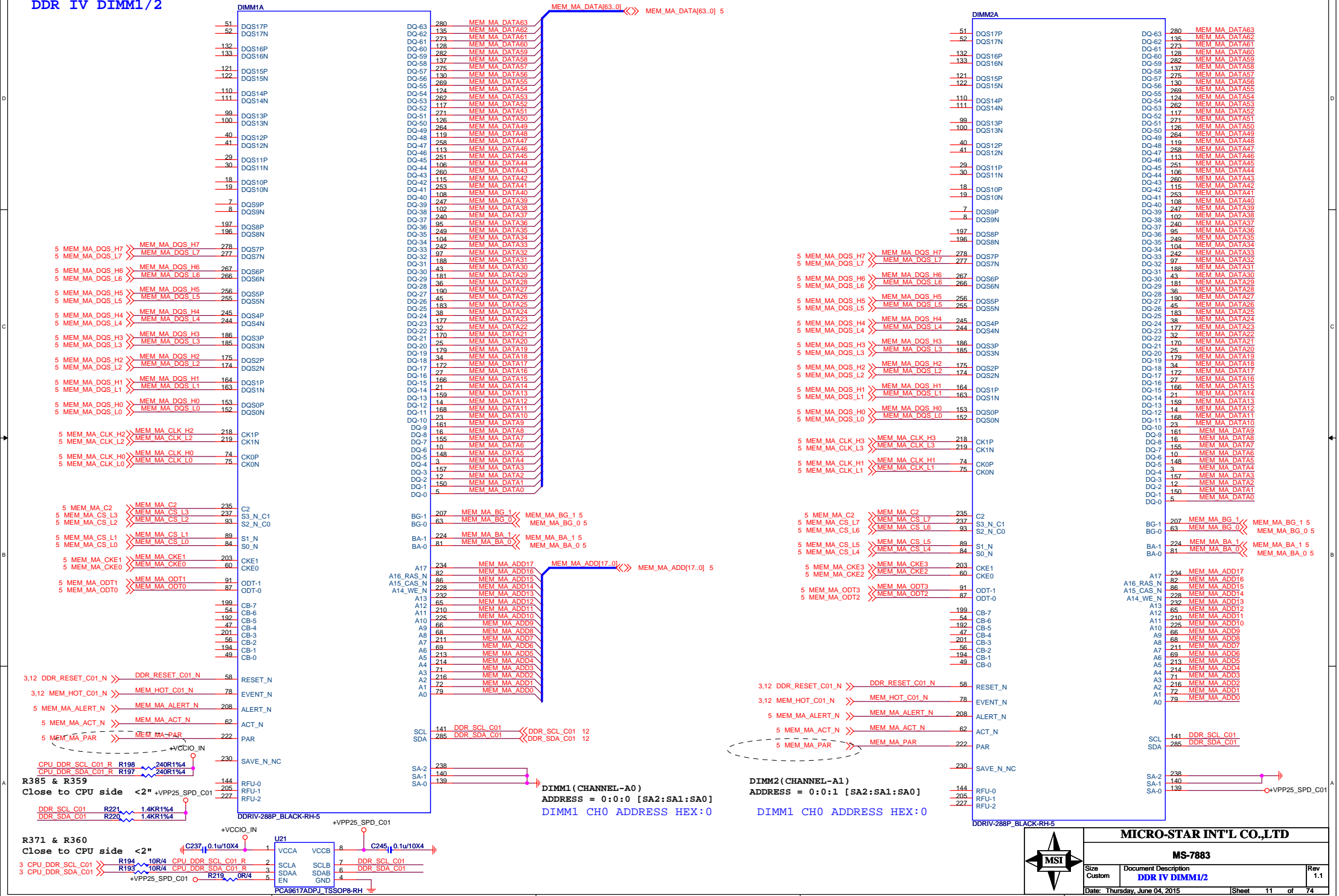
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

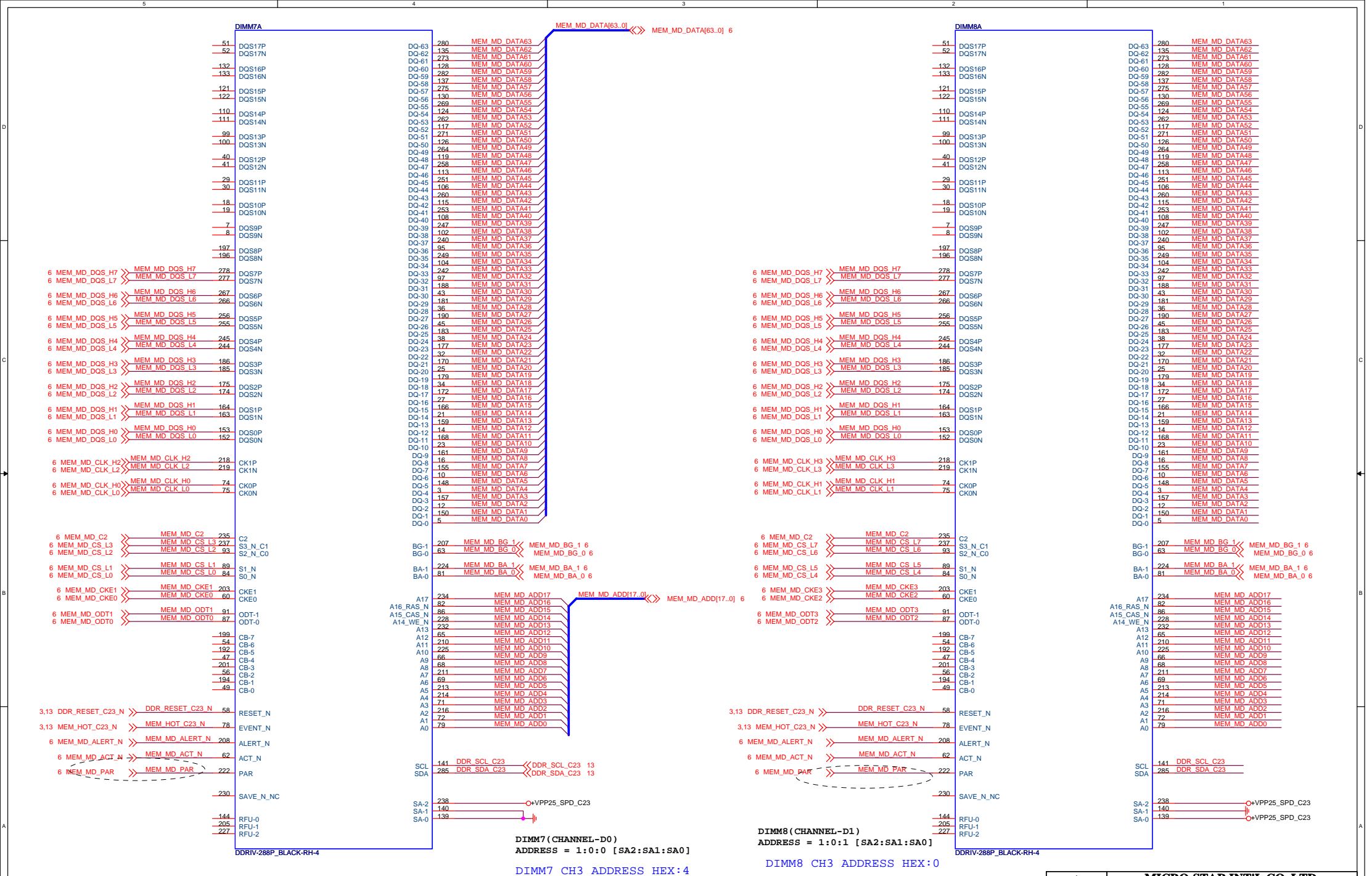




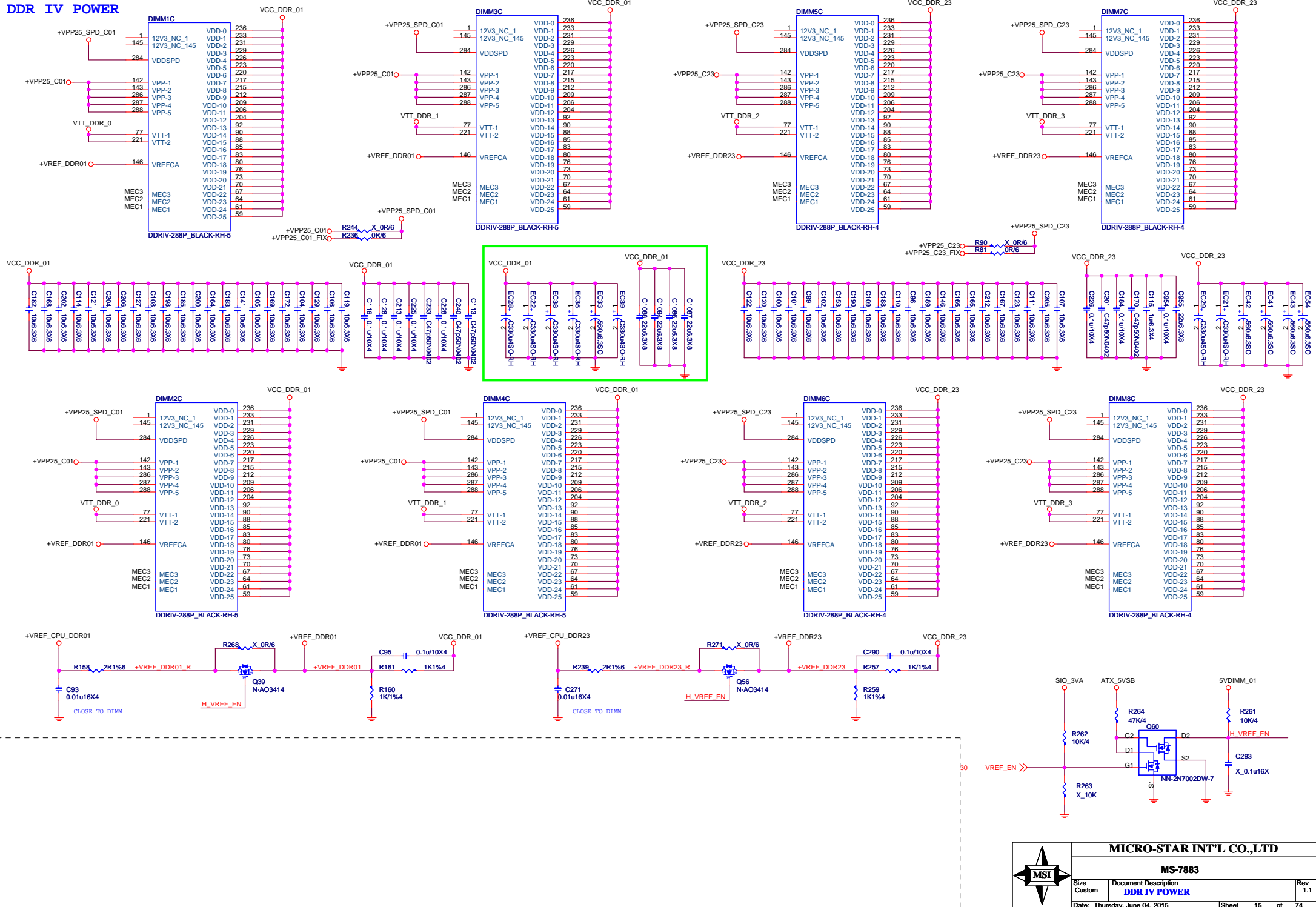


DDR IV DIMM1/2

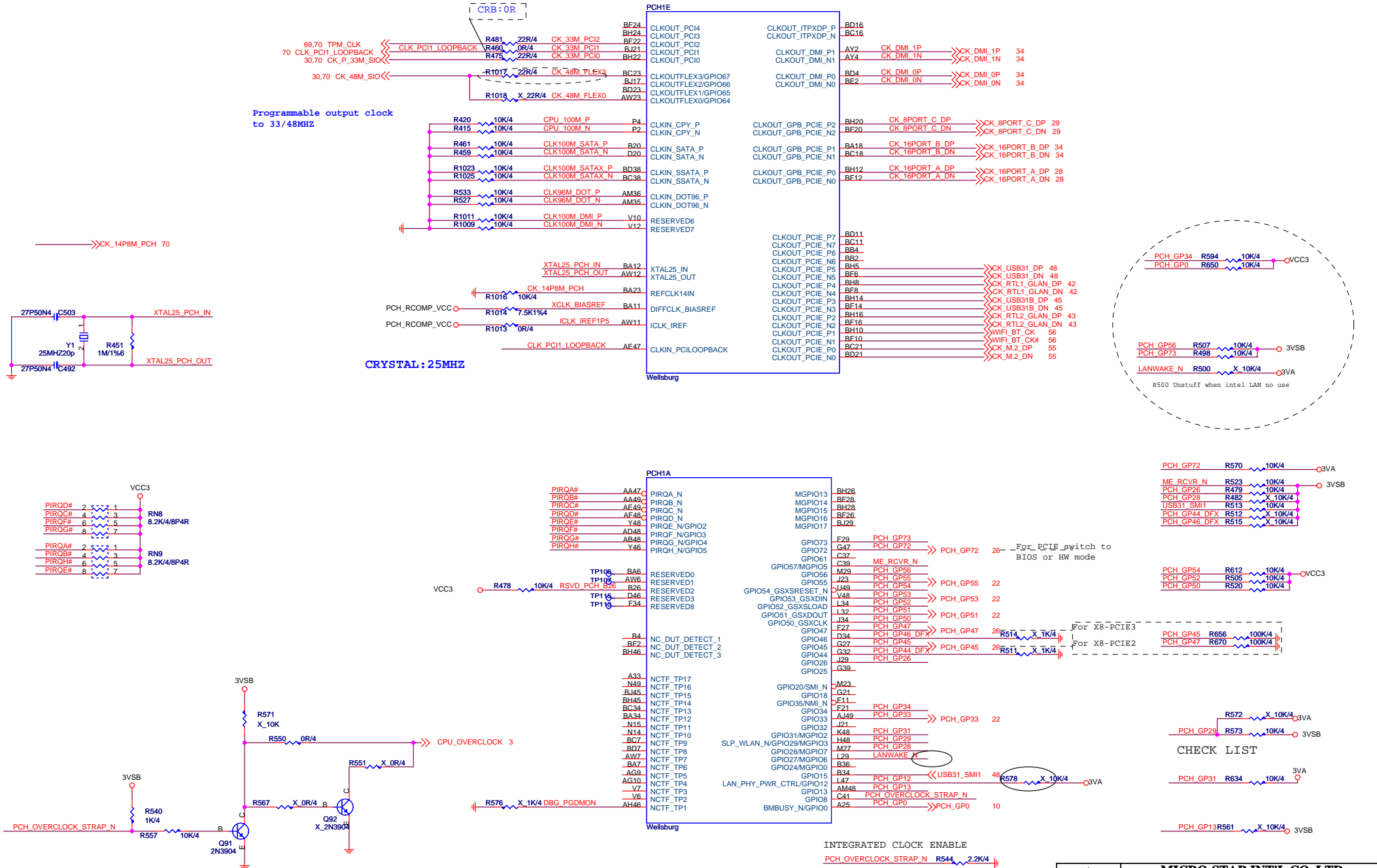




DDR IV POWER

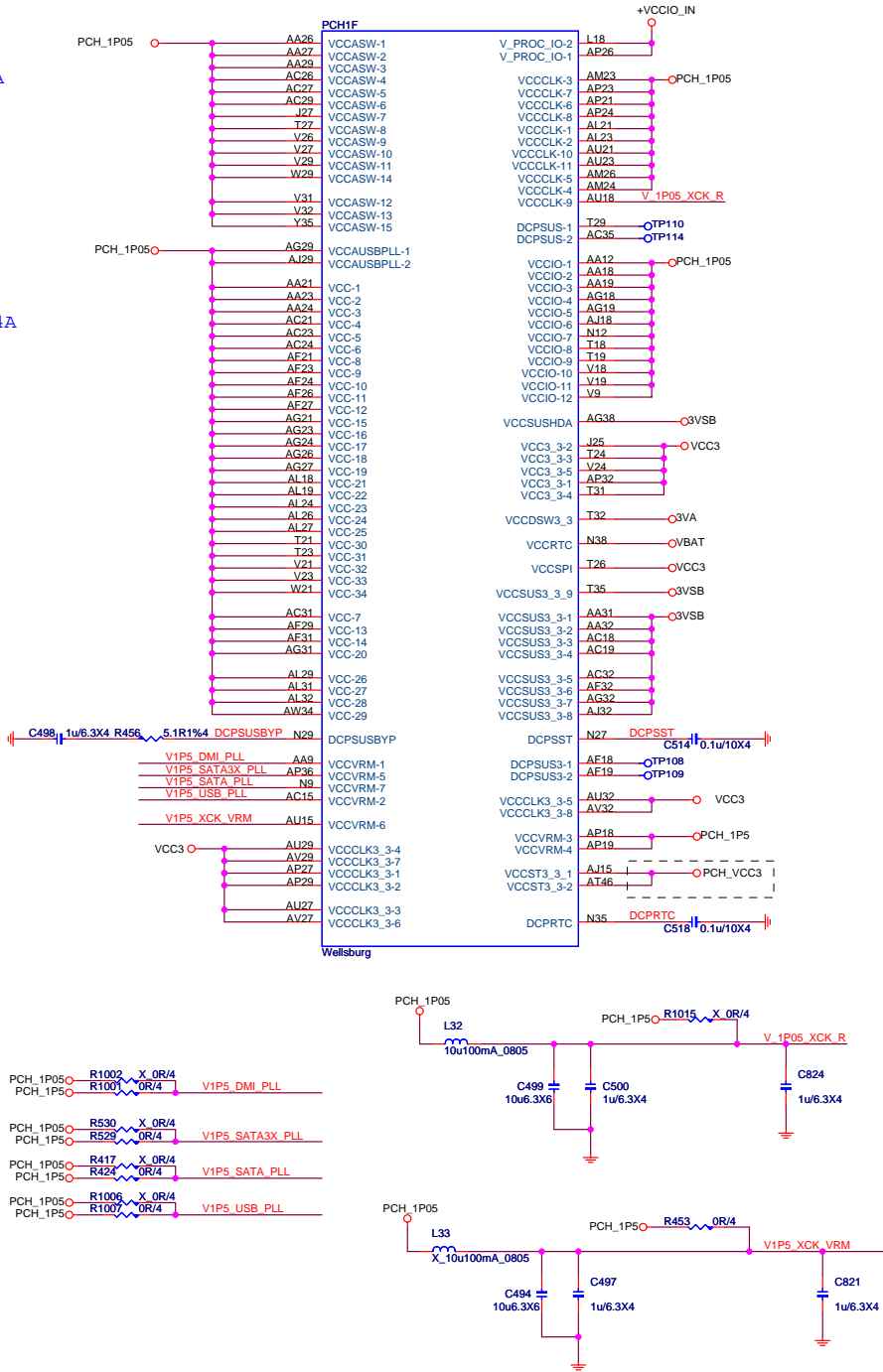


PCH-CLK/GPIO

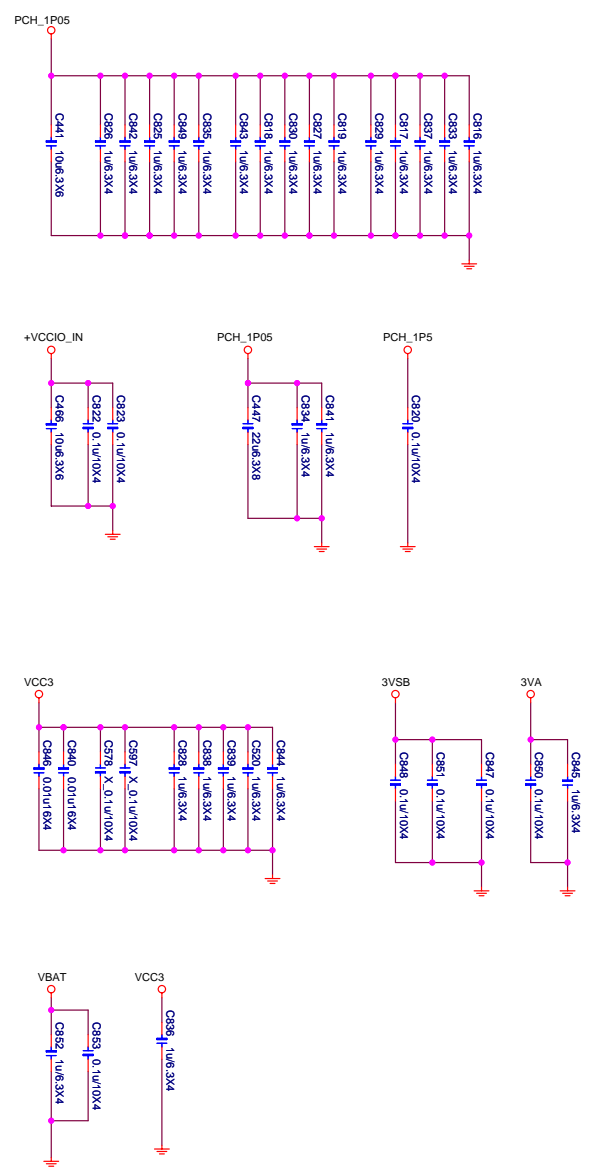


PCH-POWER

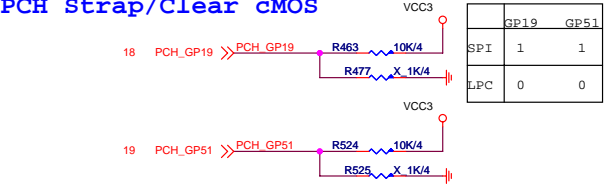
PCH_1P05:5.83A
+1P05V_ME:0.67A
VCC3:0.2A
3VSB:0.27A
SPI_VCC3:0.02A
3VA:0.02A
+VCCIO_IN:0.004A



PCH decoupling cap



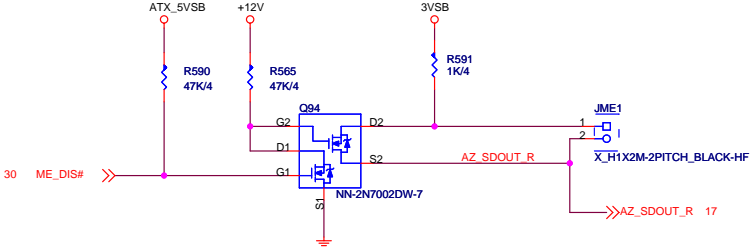
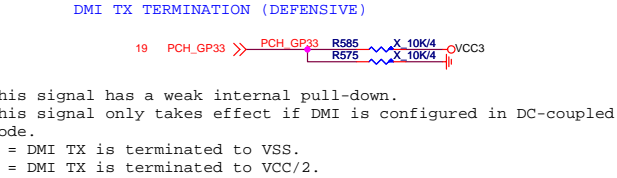
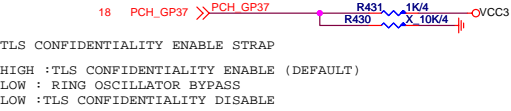
PCH Strap/Clear CMOS



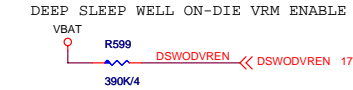
DMI RX Termination

18 PCH_GP36 >> PCH_GP36

This signal has a weak internal pull-down.
This signal only take effect if DMI is configured in AC-coupled mode.
0 = DMI RX is terminated to VSS.
1 = option not supported.



HIGH (1-2):SECURITY MEASURES OVERRIDEN
LOW (0-1) : SECURITY PER FLASH DESCRIPTOR (DEFAULT)



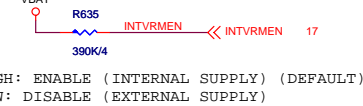
HIGH: ENABLE (INTERNAL SUPPLY) (DEFAULT)
LOW: DISABLE (EXTERNAL SUPPLY)

LOW : REBOOT
HIGH: NO-REBOOT

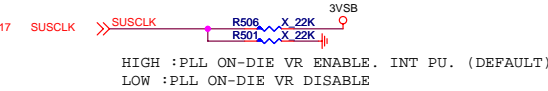
NO REBOOT OPTION STRAP



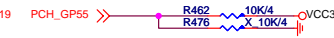
INTEGRATED SUS 1.05V VRM ENABLE



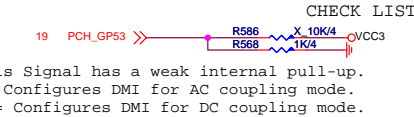
PLL ON-DIE VR ENABLE



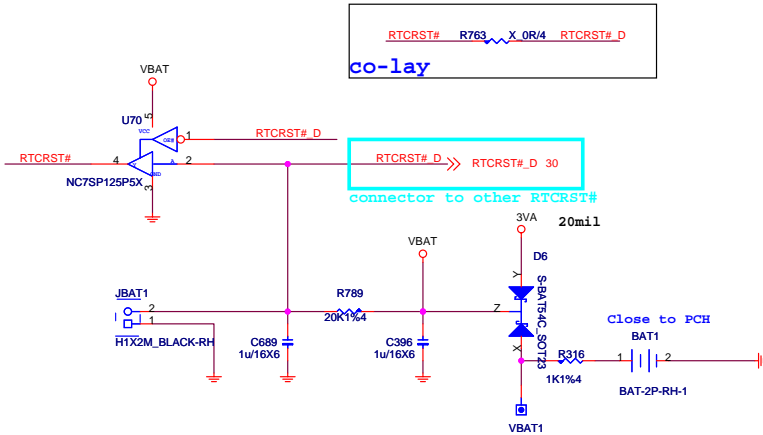
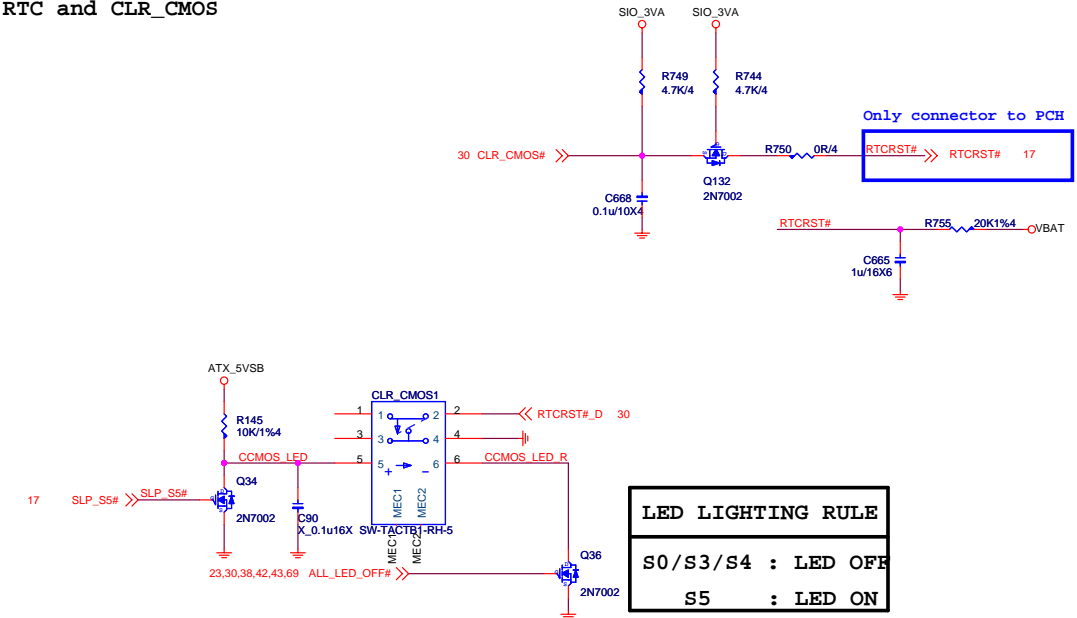
Top-Block Swap
Override



DMI AC Coupling

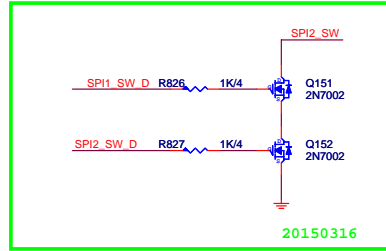
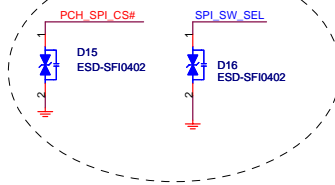


RTC and CLR_CMOS



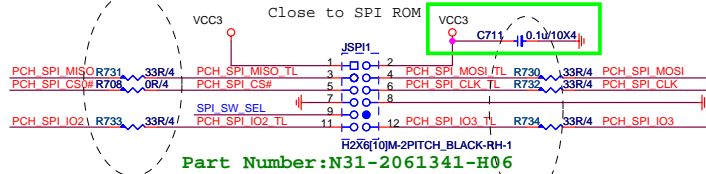
tri-state		
INPUT		outout pin4
PIN1	PIN2	
L	H	H
L	L	L
H	X	Z

17 PCH_SPI_CS0# << PCH_SPI_CS0#
17 PCH_SPI_MOSI << PCH_SPI_MOSI
17 PCH_SPI_MISO << PCH_SPI_MISO
17 PCH_SPI_CLK << PCH_SPI_CLK
17 PCH_SPI_IO2 << PCH_SPI_IO2
17 PCH_SPI_IO3 << PCH_SPI_IO3

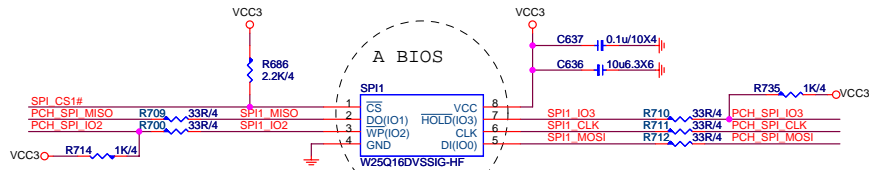


SPI DEBUG PROT

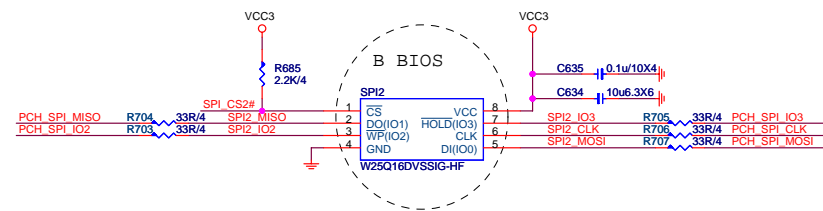
Close to SPI ROM



17 PCH_PWROK >> PCH_PWROK R1065 0R/4 SPI_SW_SEL
2014.06.05 Add for support TL624-1.1



16M ROM



SPI FLASH ROM

Place close to SB.

*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
*SPI_CLK & SPI_CS# must be length matched to within 500mils.

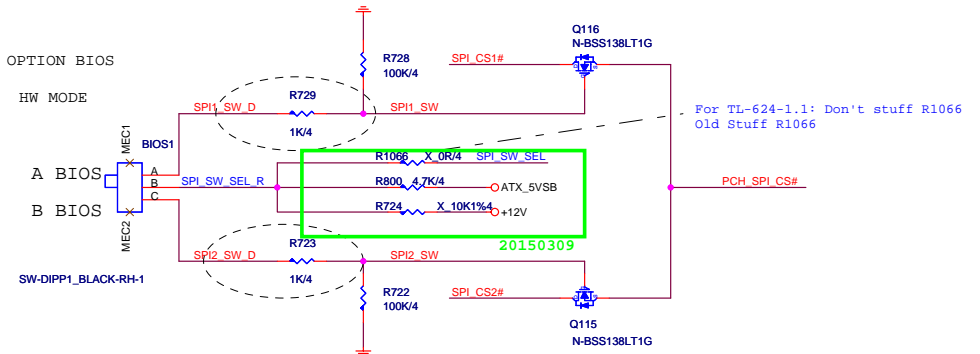
OPTION BIOS

HW MODE

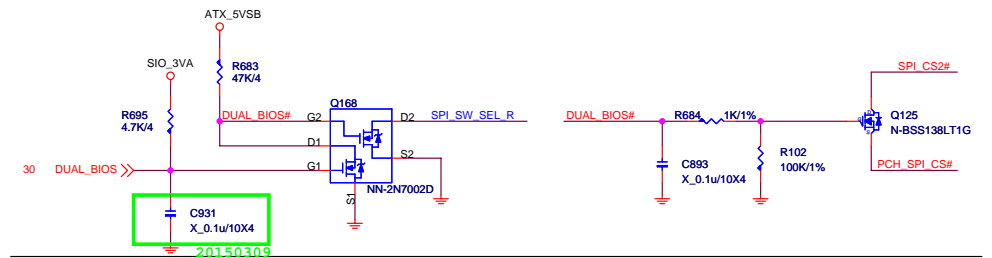
A BIOS

B BIOS

SW-DIPP1_BLACK-RH-1



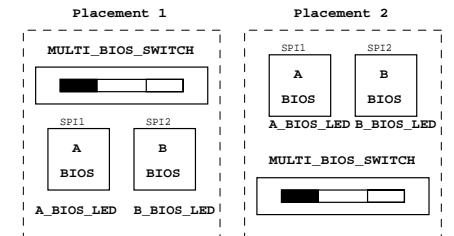
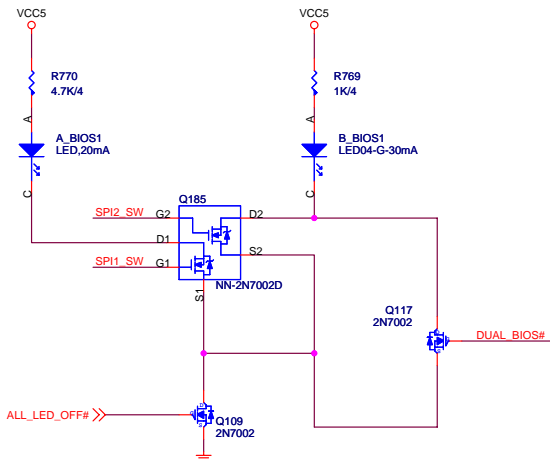
For auto testing in factory. Modify 2014.12.18



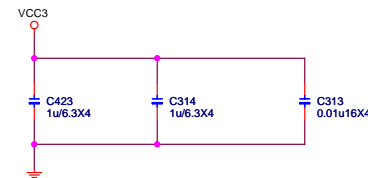
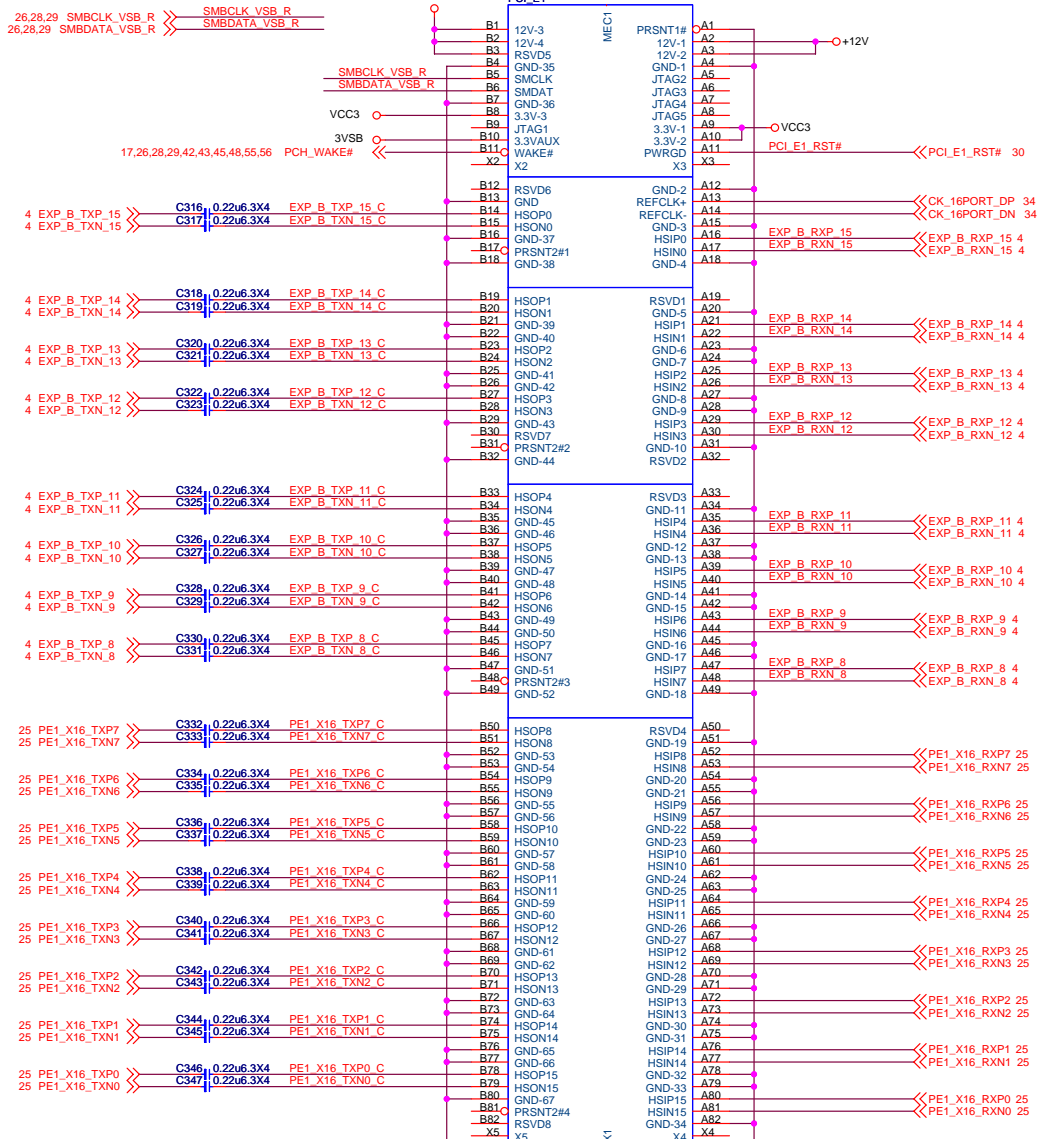
* if you not support Standby power in S5 Status, component "MULTI_BIOS_SWITCH1.B(PIN B)" Pull-high to +12V & Q12/Q13 MOS select 2N7002

* if you support Standby power in S5 Status(Ex: PCH is B75 Chipset), component "MULTI_BIOS_SWITCH1.B(PIN B)" pull-igh to ATX_5VSB, component Q12/Q13 must select "Vth" under 1V (Component Suggestion as below)

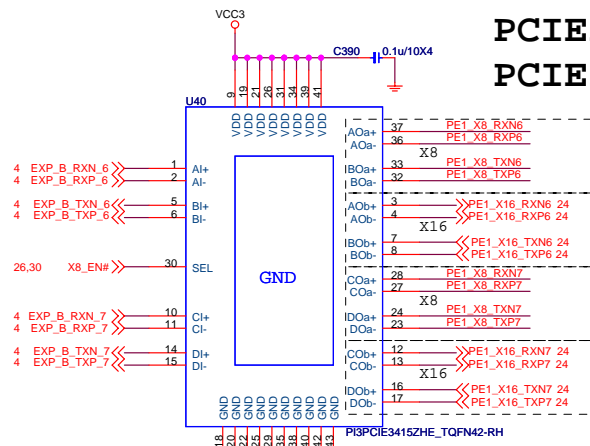
D03-0341409-A68 / D03-0230019-A30



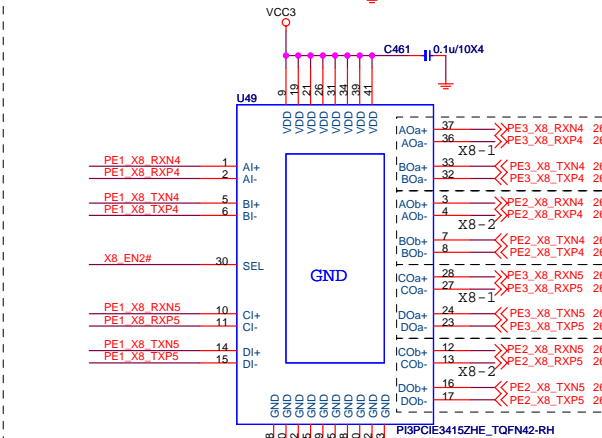
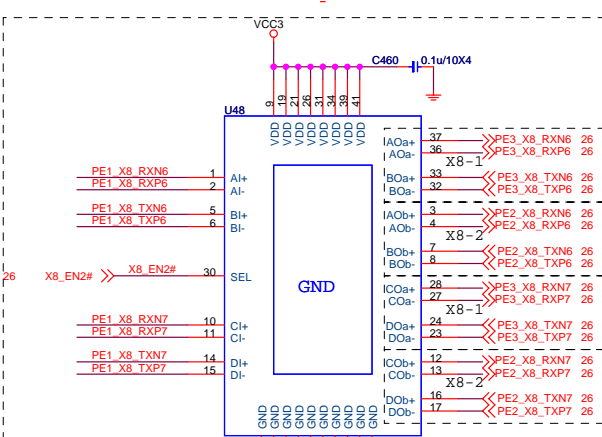
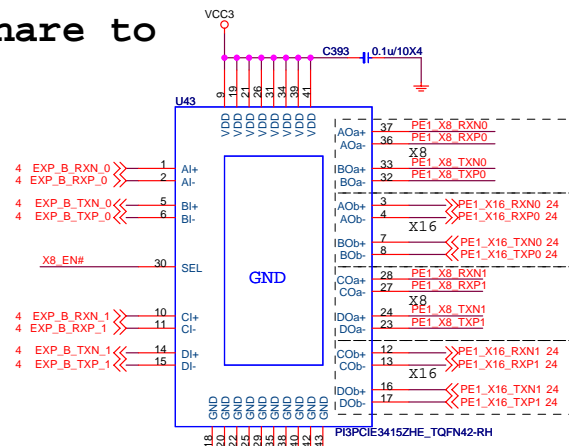
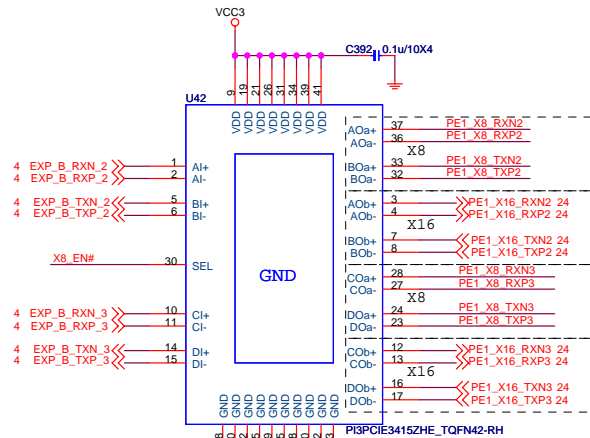
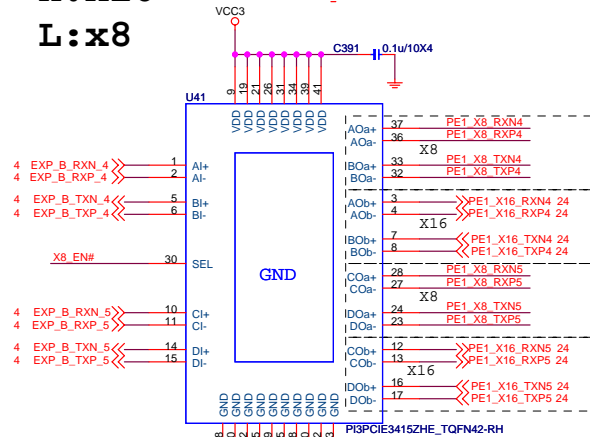
PCIE1(X16) & PCIE2(X1) Slots



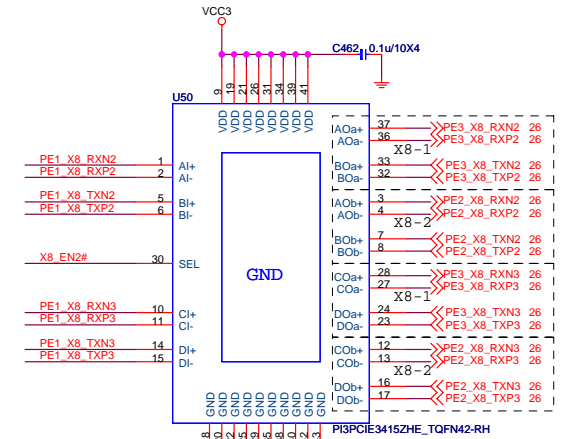
PCIE1(x16) share to PCIE2(x8)



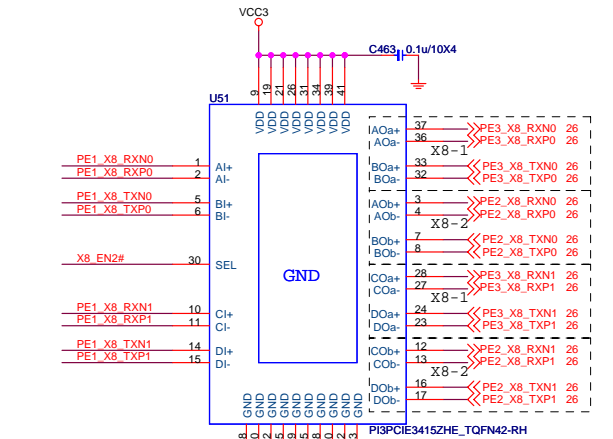
H:x16
L:x8



Switch PCIE(x8) for PCIE2 or PCIE3



H:x8-E2
L:x8-E3



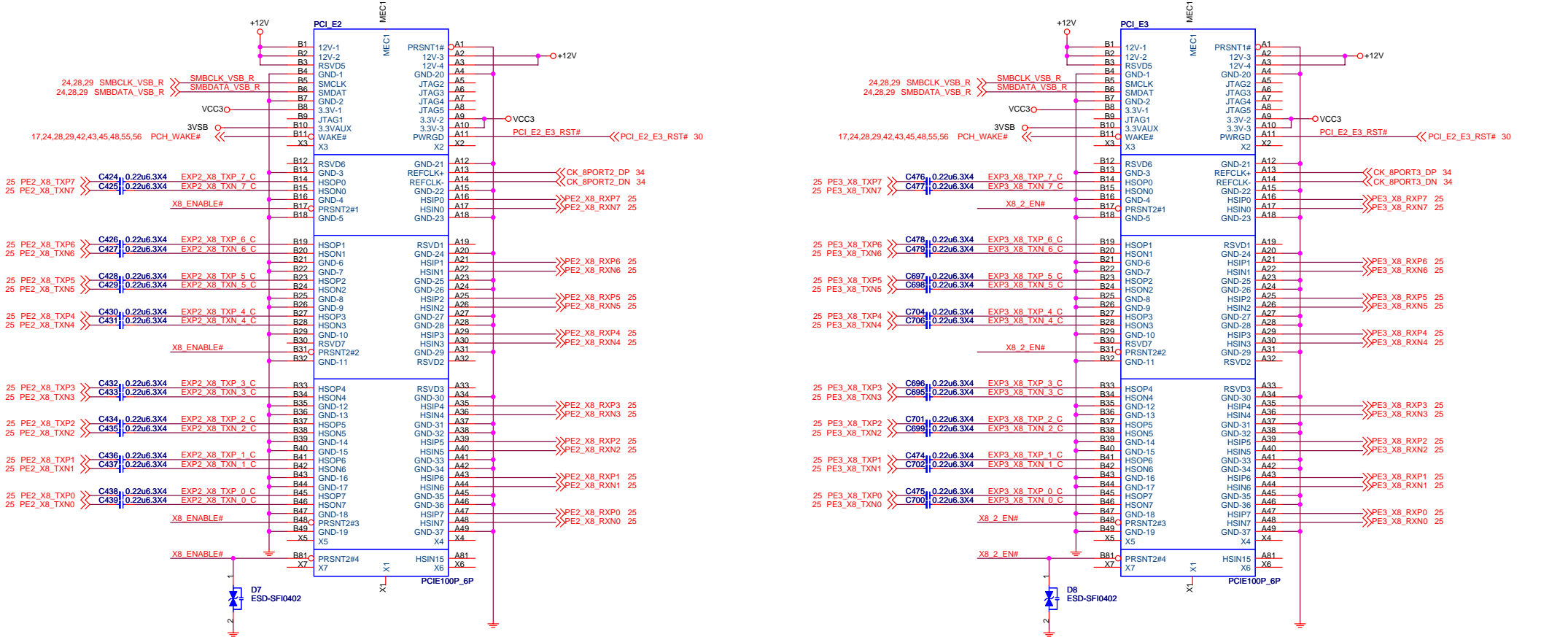
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MS-7883

Size Custom Document Description PCIE Switch 3415 Rev 1.1

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PCIE5(X8) /PCIE3415



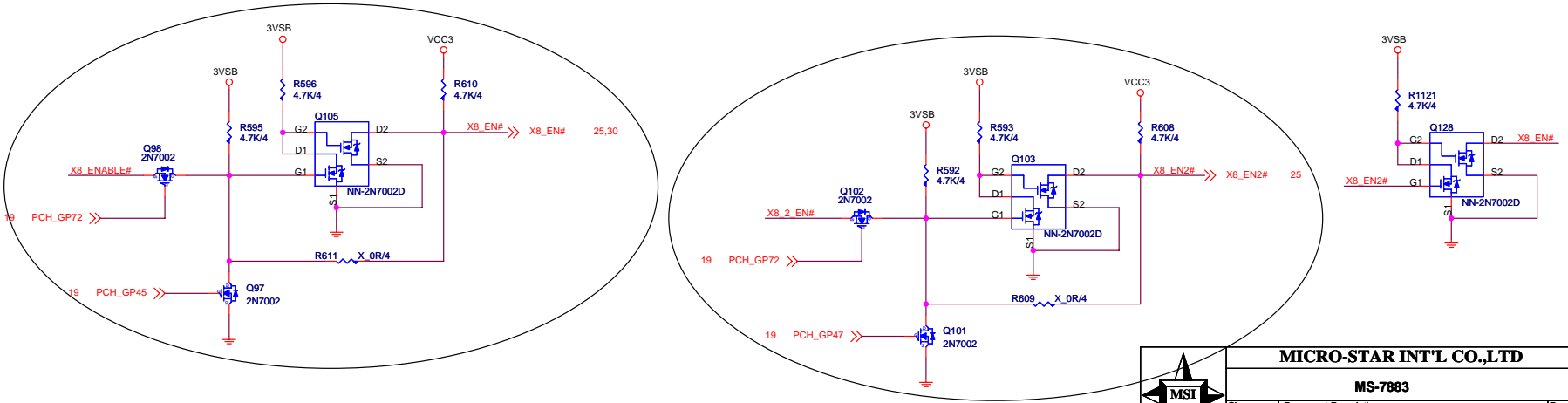
GPIO72

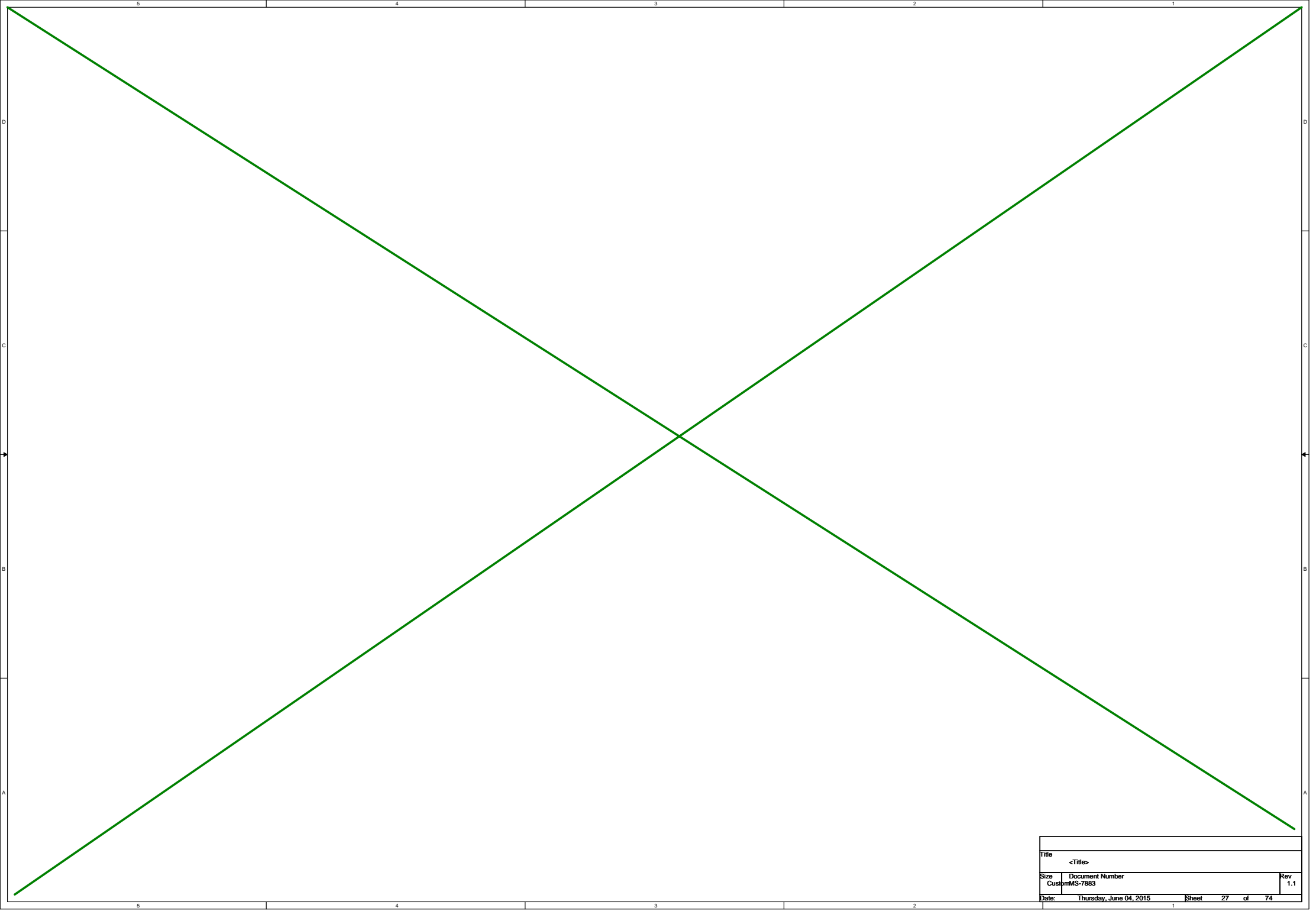
- 0: BIOS MODE
- 1: HW MODE

If USE HW MODE
PCH_GPIO45/47 programming to GPI
PCH_GPIO72 programming to GPO

If USE BIOS MODE
PCH_GPIO45/47 programming to GPO

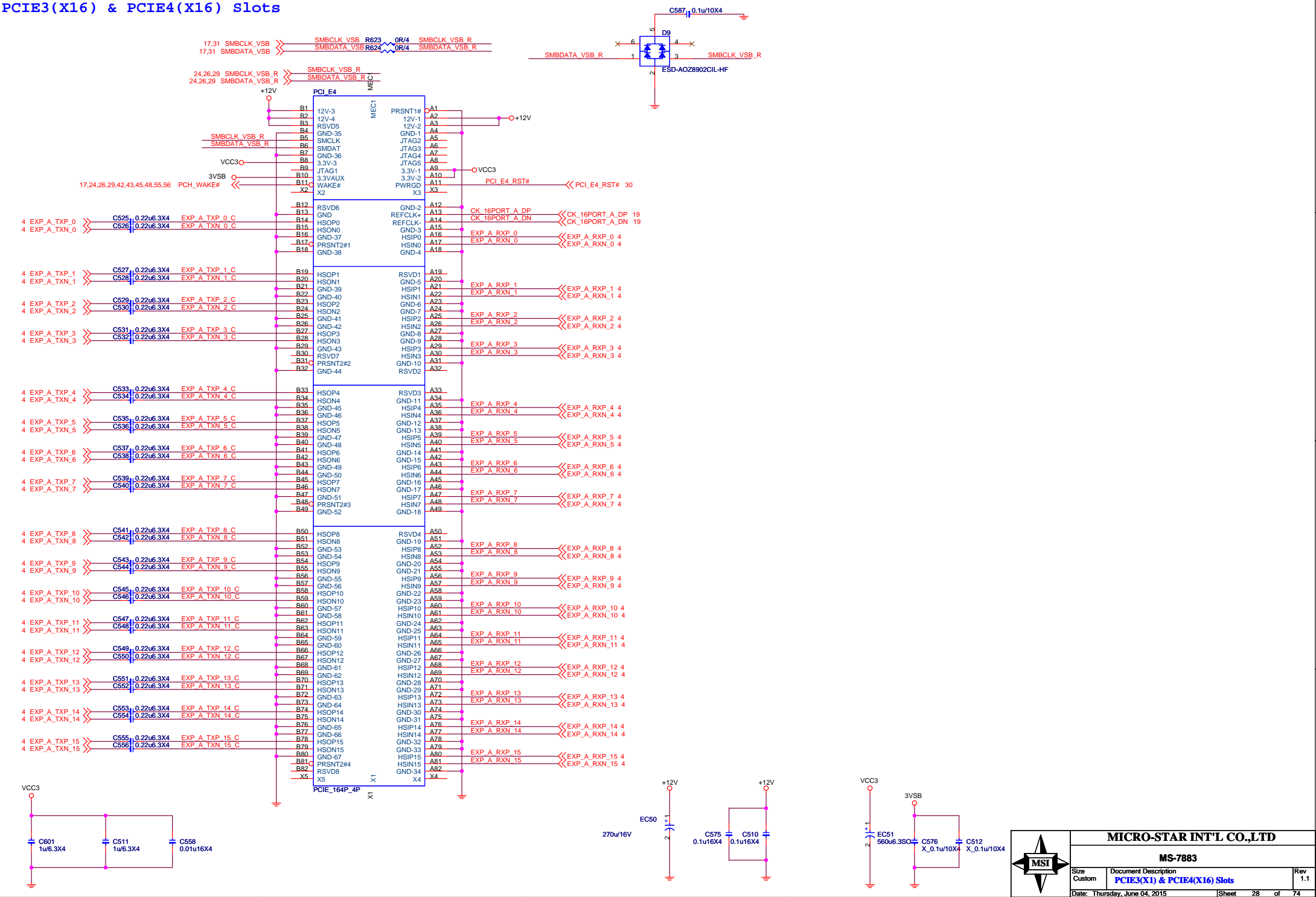
PCH Status	GPIO72	GPIO45	GPIO47
AUTO	1	GPI(def:0)	
16,0,0	0	X	X
8,8,0	0	1	0
8,0,8	0	0	1



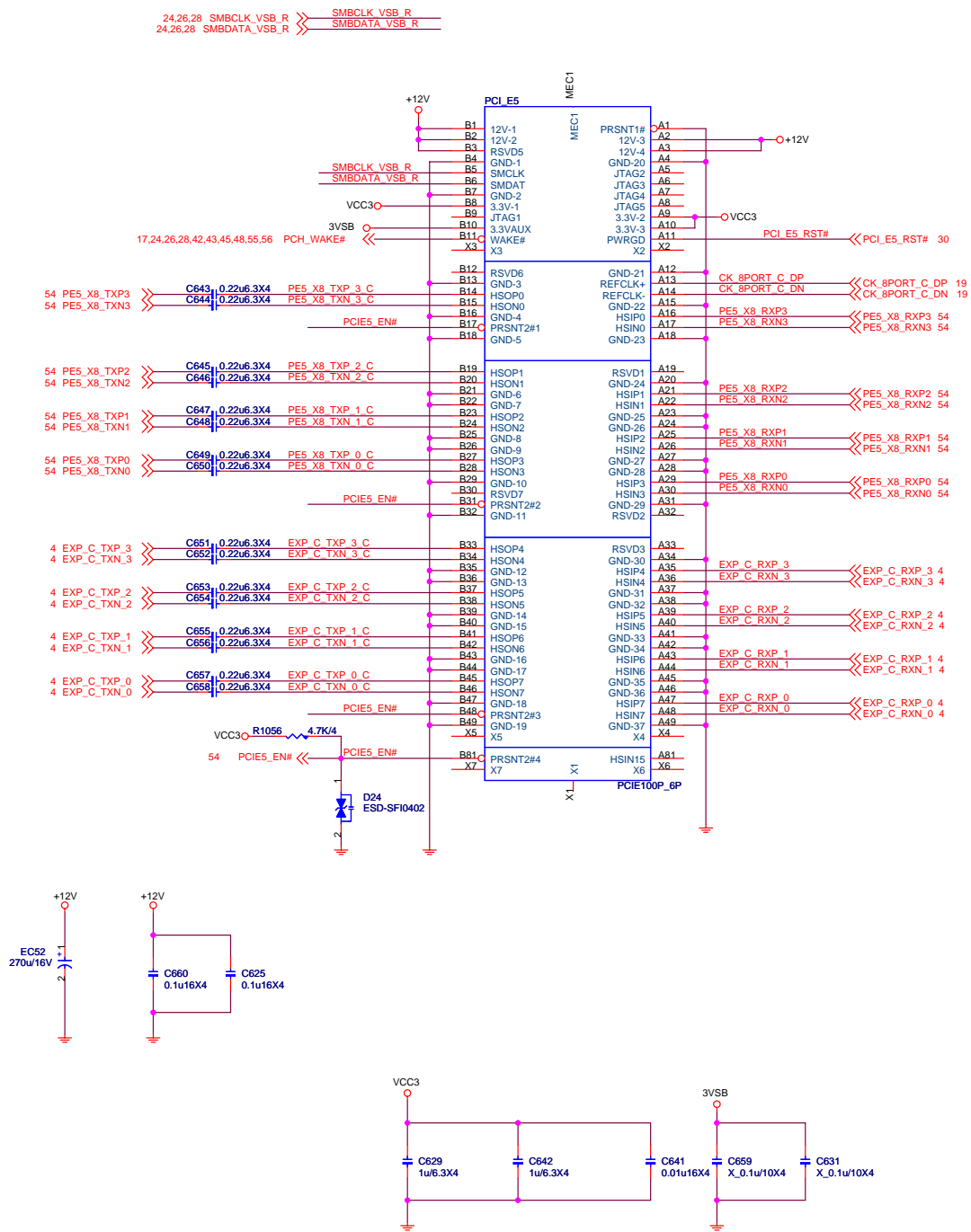


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Custom	MS-7883	1.1
Date:	Thursday, June 04, 2015	Sheet 27 of 74

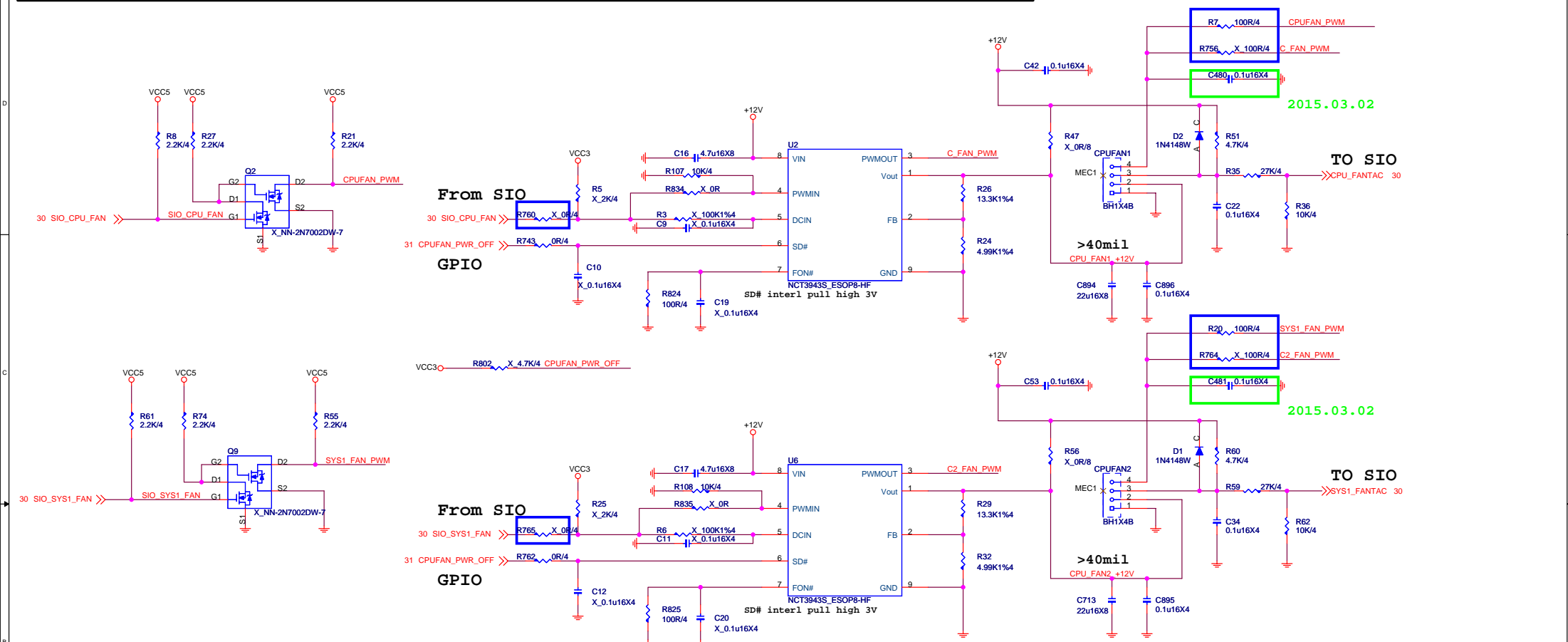
PCIE3(X16) & PCIE4(X16) Slots



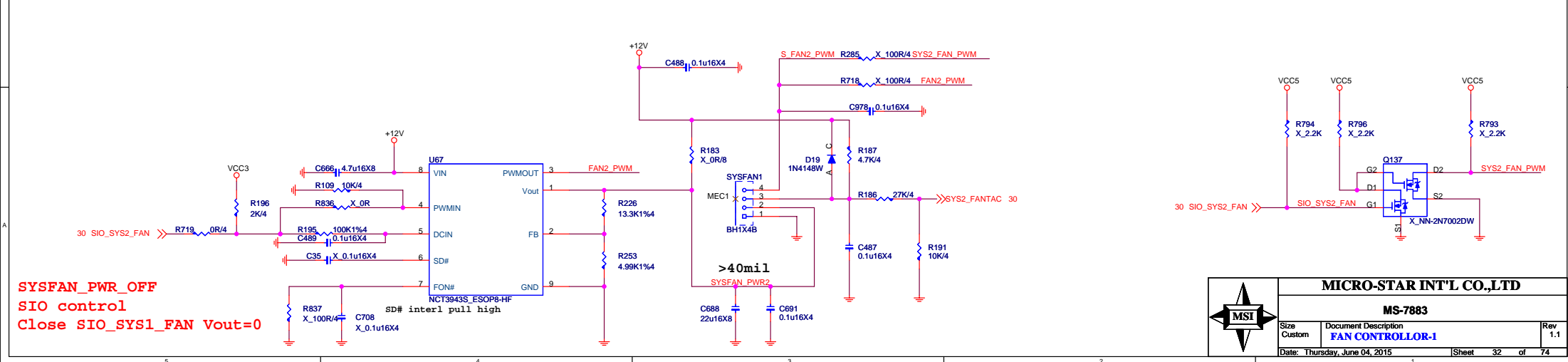
PCIE5(X8) slots



Type E : 4 PIN CPU FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6792)

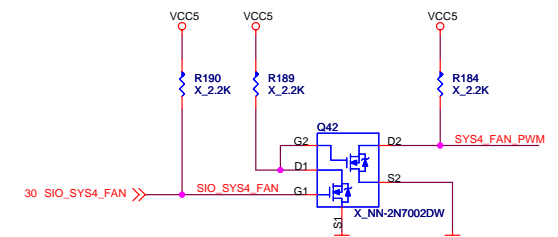
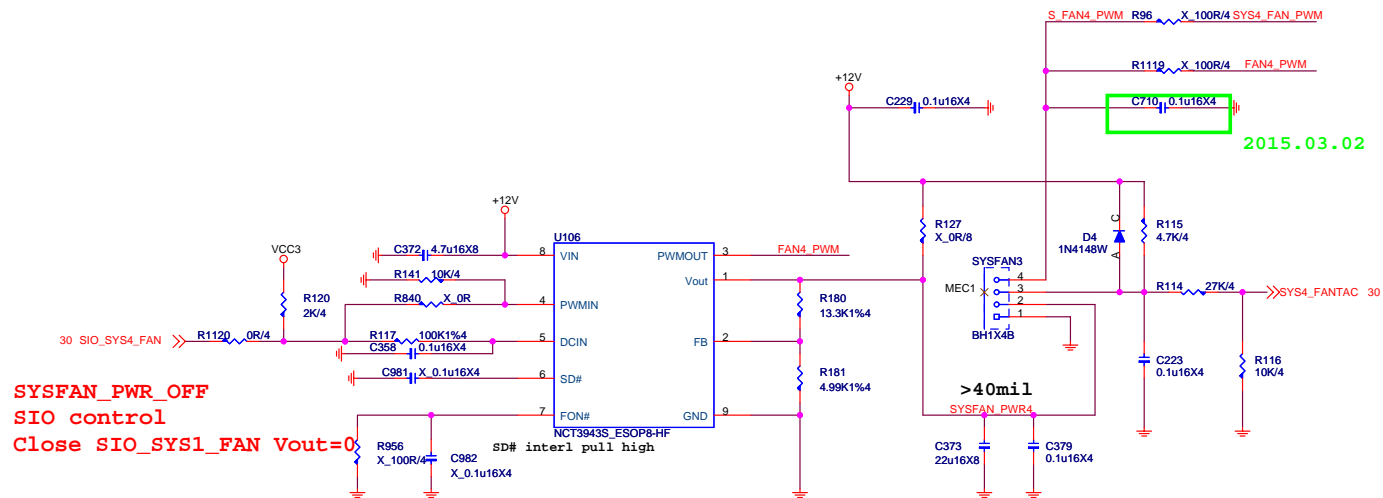
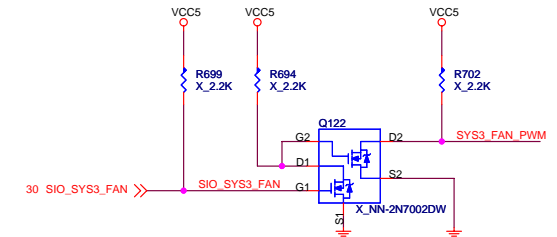
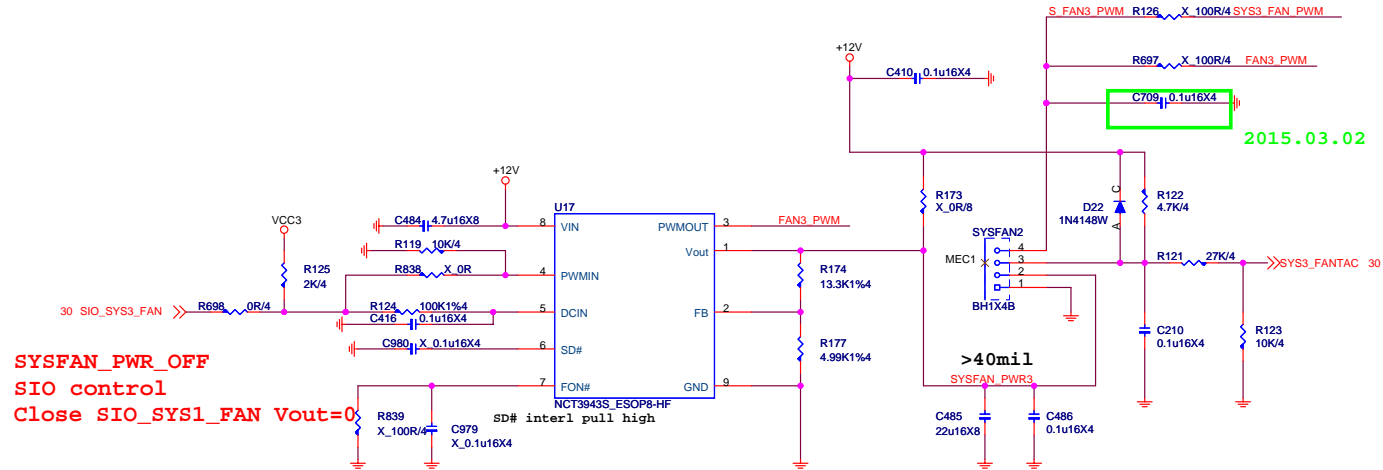


Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6792)

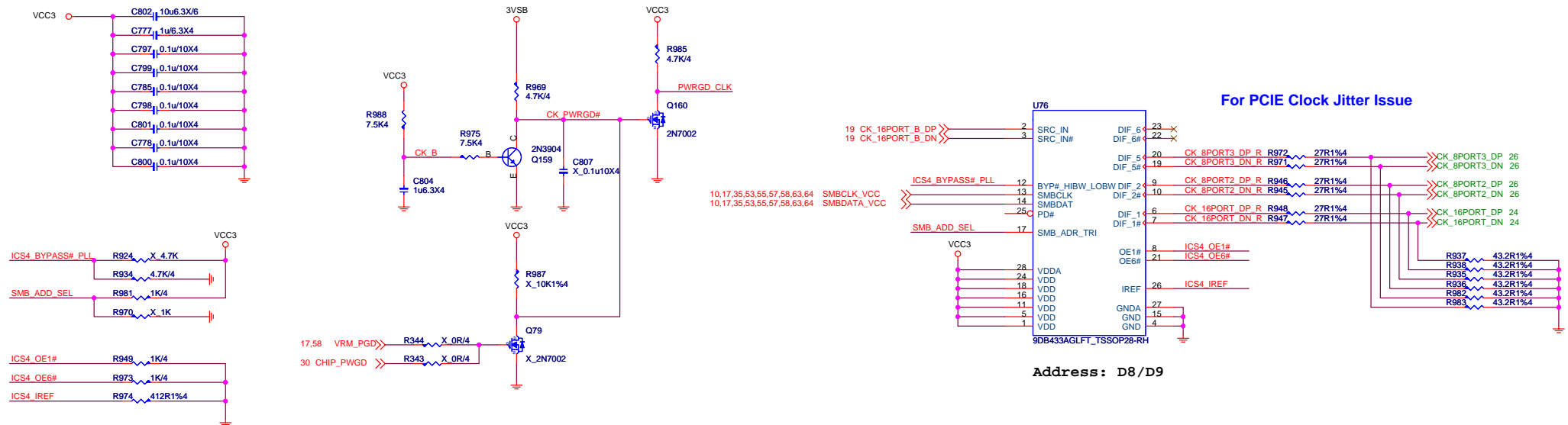


SYSFAN_PWR_OFF
SIO control
Close SIO_SYS1_FAN Vout=0

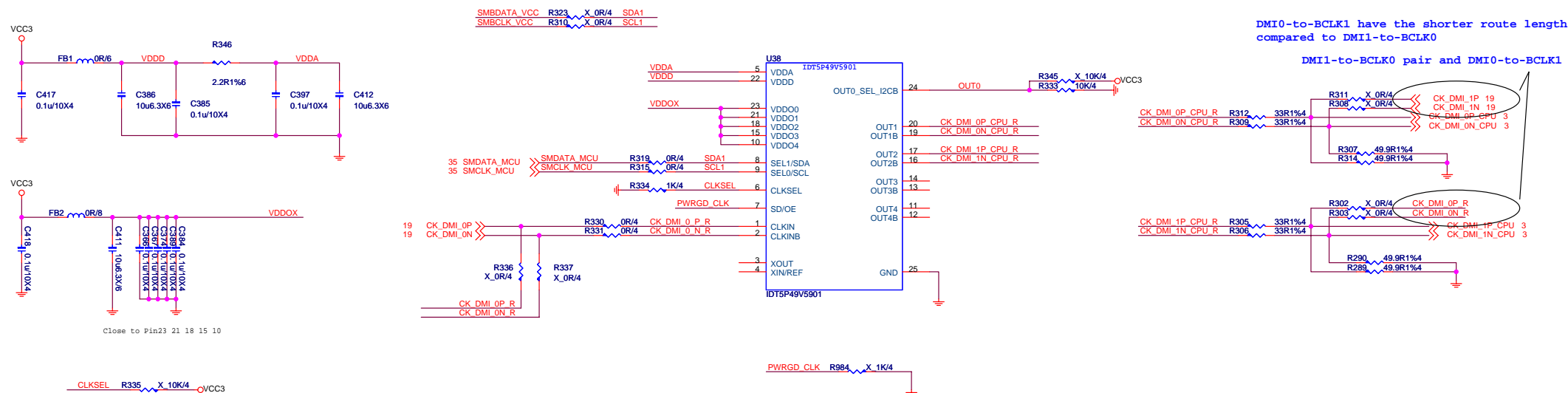
Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6792)



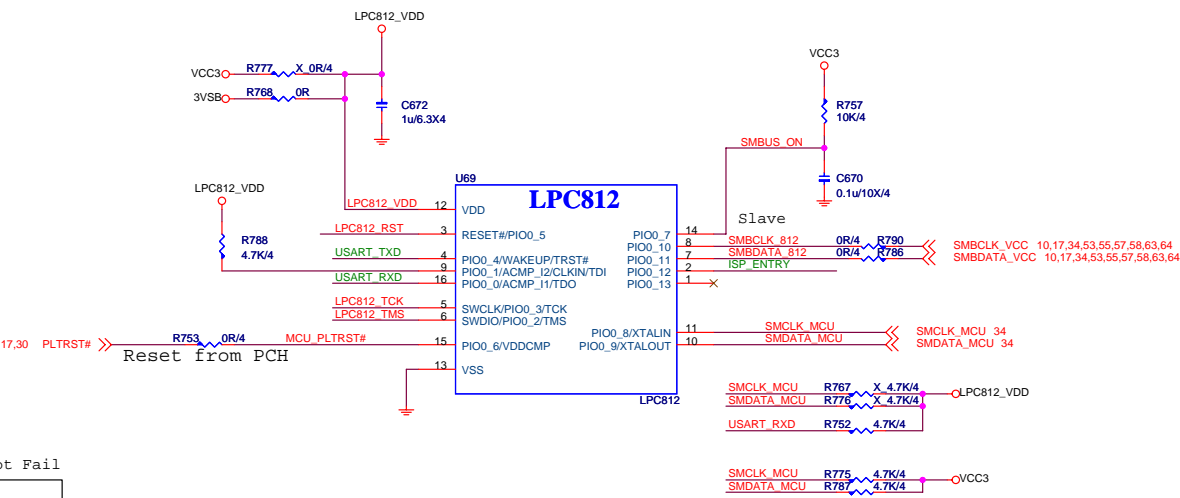
CLK Buffer_9DB433



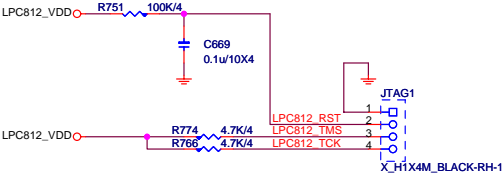
CLK GEN-IDT5P49V5901



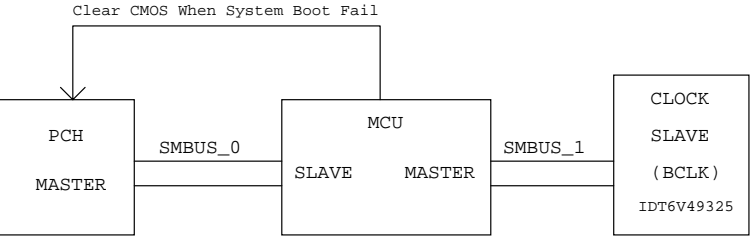
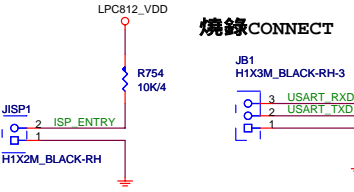
SIO 6792 , GPIO13
default low , active high



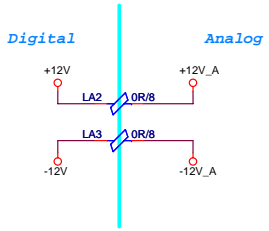
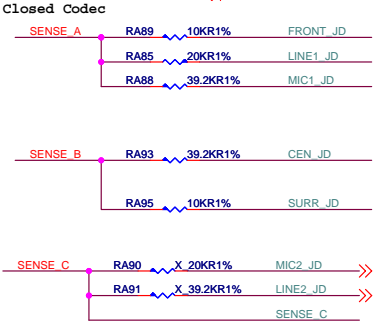
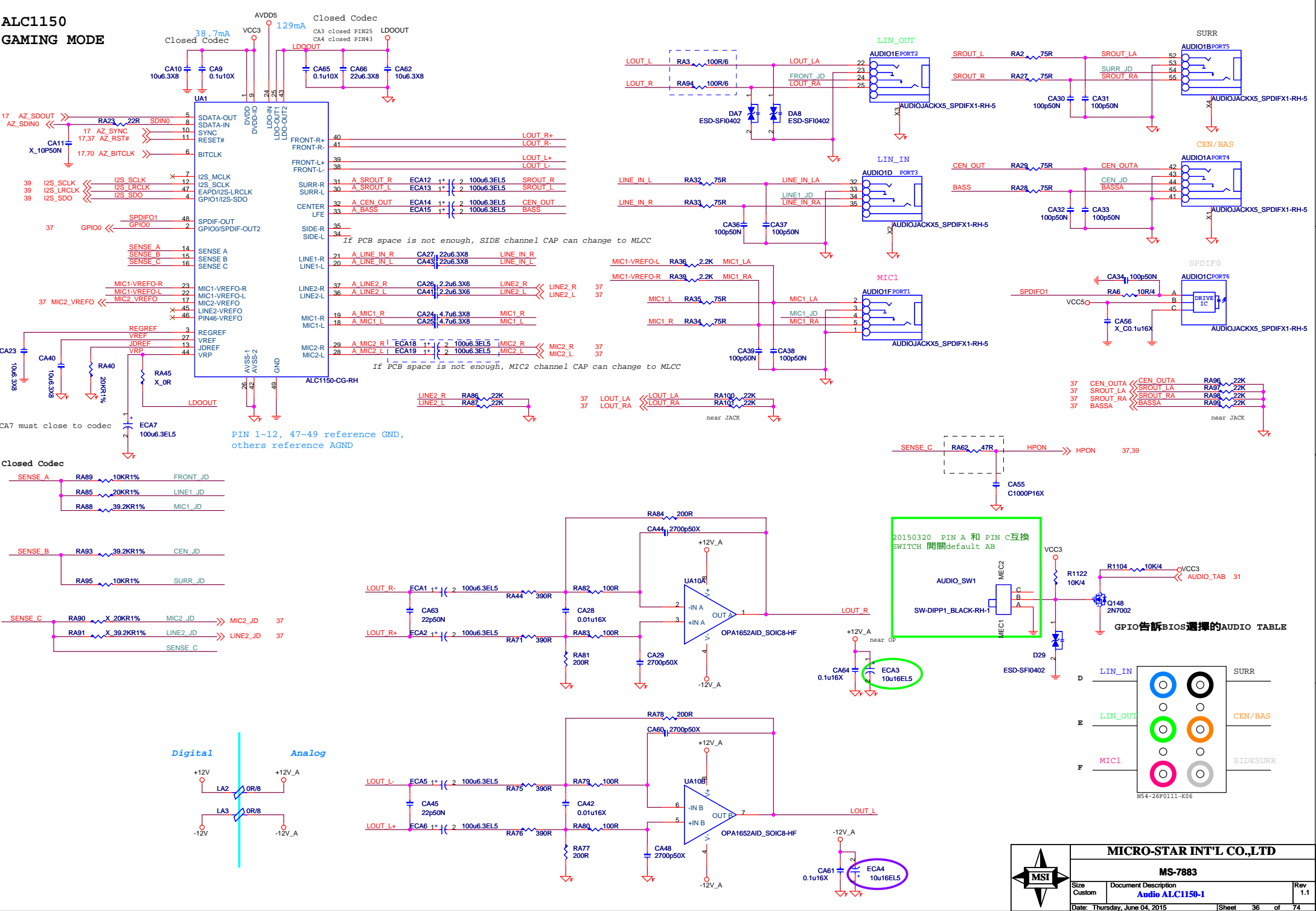
JTAG for SW DEBUG



燒錄CONNECT



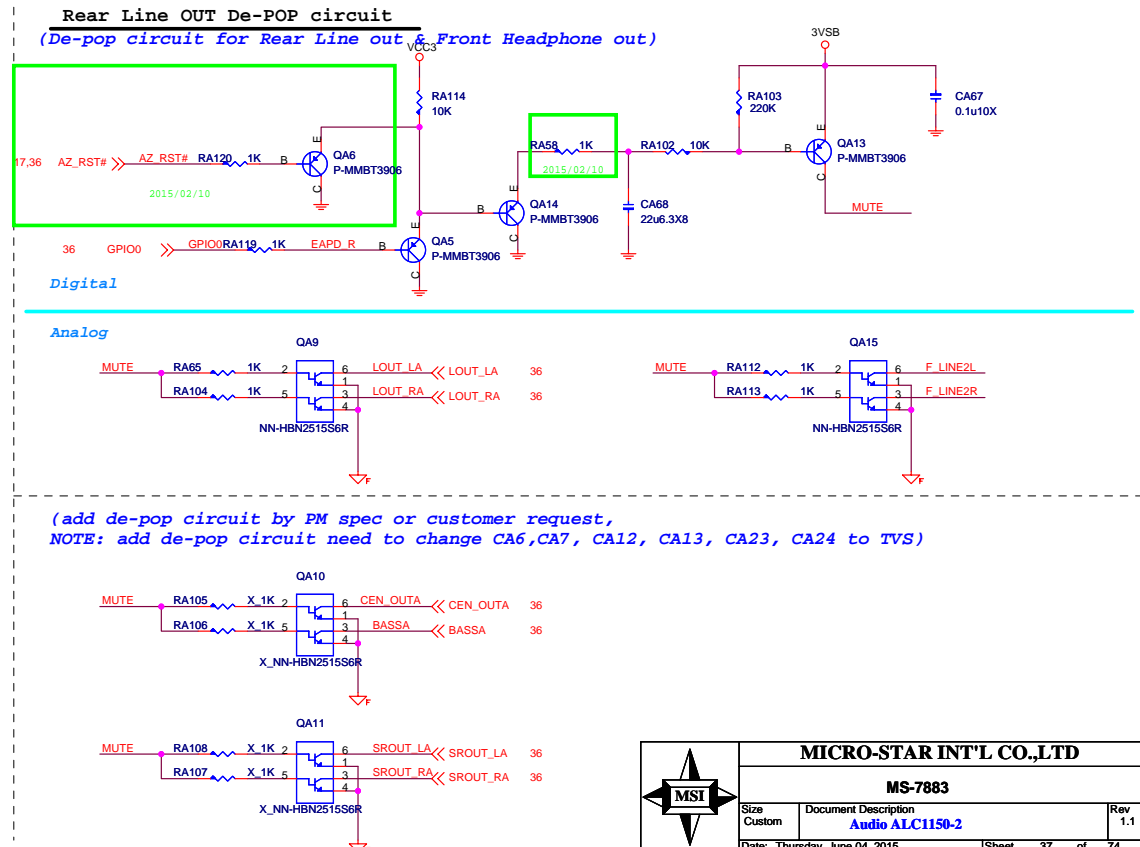
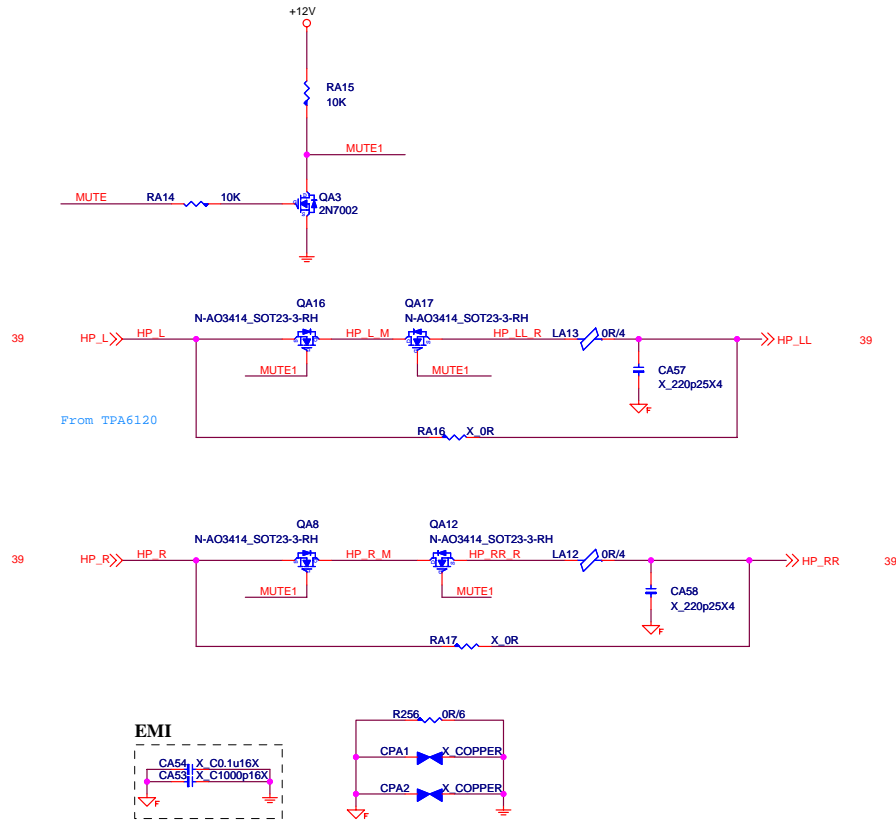
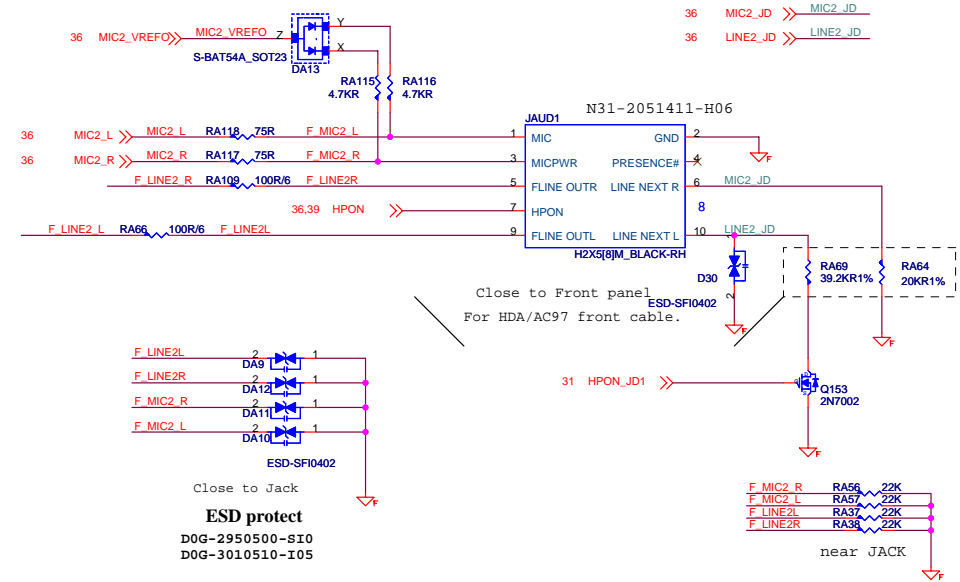
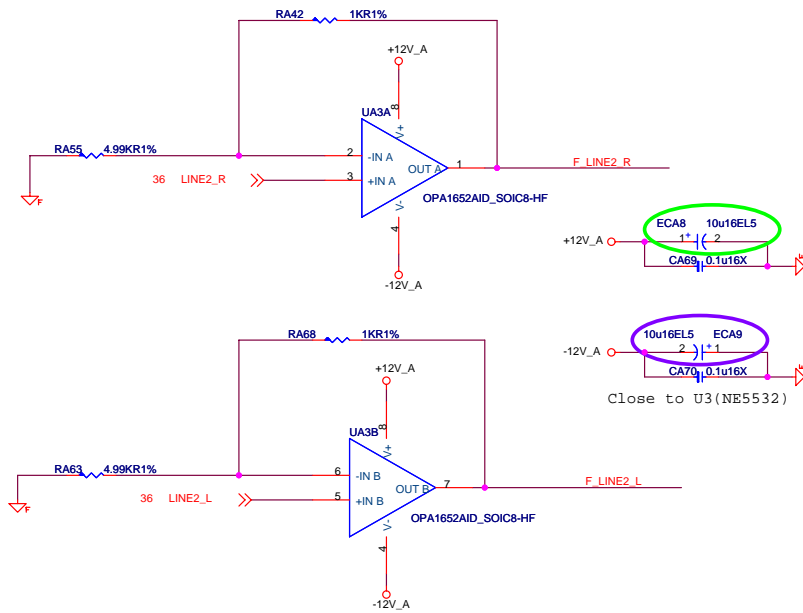
ALC1150
GAMING MODE



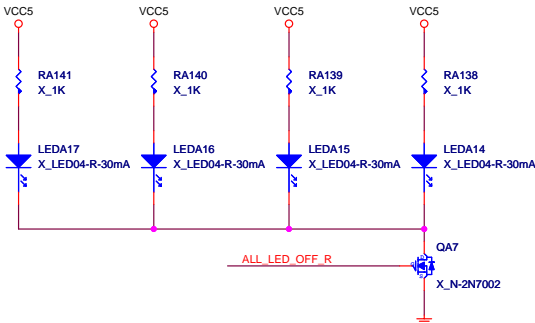
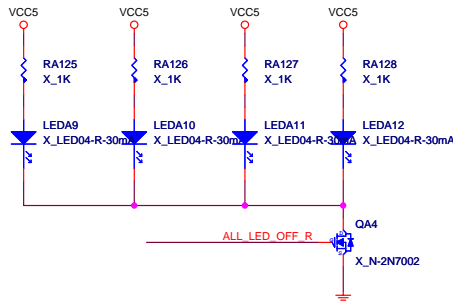
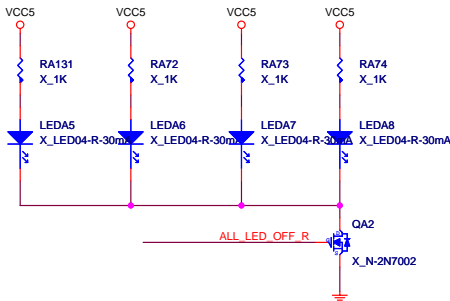
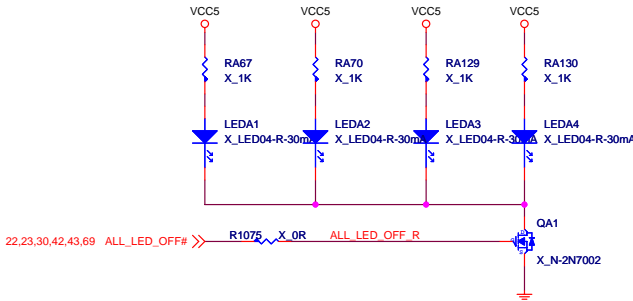
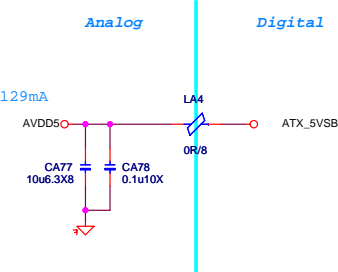
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Audio moat is transparent and width 40mil



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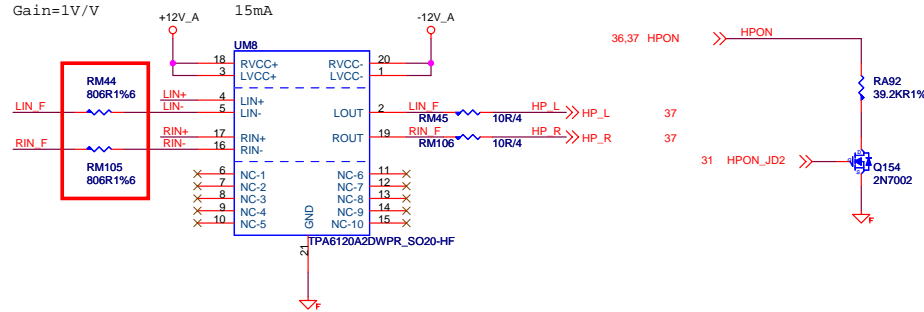
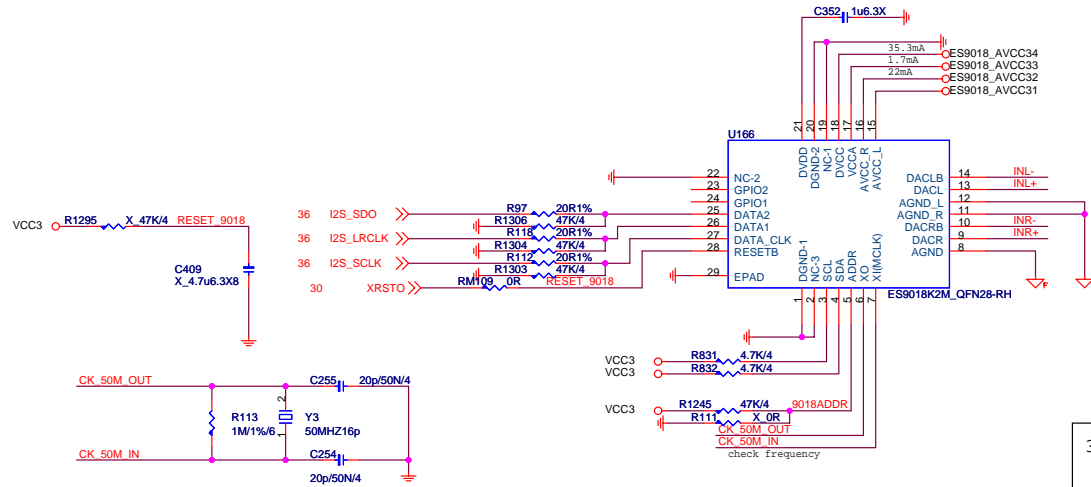
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Size	Document Description	Rev
Custom	Audio power/LED	1.1
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ADDR	CHIP ADDRESS
0	0x90
1	0x92

AVCCDAC3.3(MCLK=50MHz, Fs=192kHz):max W=71.5mW, I=21.667mA
 DVCC3.3(MCLK=50MHz, Fs=192kHz):max W=116.48mW, I=35.3mA
 VCCA3.3(MCLK=50MHz, Fs=192kHz):max W=5.5mW, I=1.667mA
 DVDD1.2:max I=0A
 Total(MCLK=50MHz, Fs=192kHz):max W=193.48mW, I=58.63mA

MVCC3:35.3mA
 M_AVCC3:23.7mA



ESS9016 Vrms = 2V
 When Vrms > 4V, TVS need > Vrms 4V

	Gain=1 Vrms=2	Gain=1.5 Vrms=3	Gain=2 Vrms=4
32 ohm	125mW	281.25mW	500mW
320 ohm	12.5mW	28.125mW	50mW
600 ohm	6.67mW	15mW	26.67mW

Po = (V^2)/R
 12.5mW < Po < 100mW

ESS9016 Vrms = 0.8V

	Gain=1.5 Vrms=1.2
32 ohm	45mW

ESS9016 Vrms = 1V

	Gain=1.5 Vrms=1.5
32 ohm	70.32mW

ESS9016 Vrms = 1.1V

	Gain=1.5 Vrms=1.65
32 ohm	85.08mW

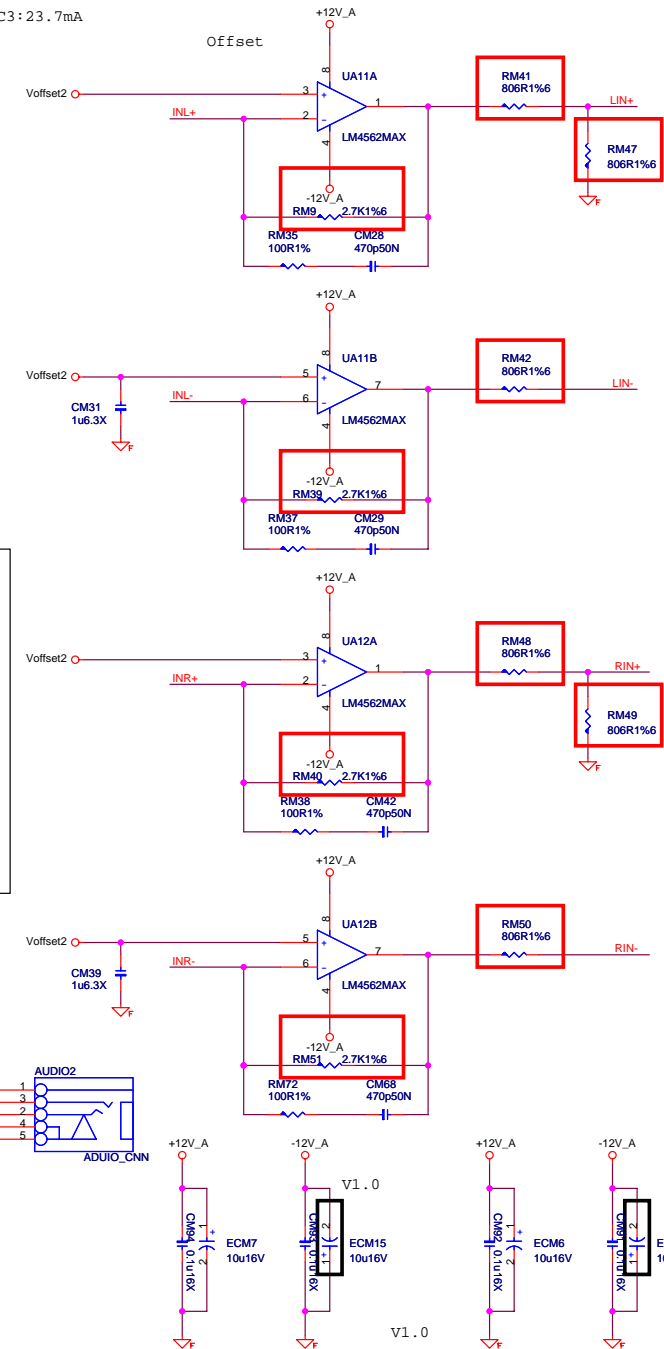
ESS9016 Vrms = 1.15V
 Sony suggest

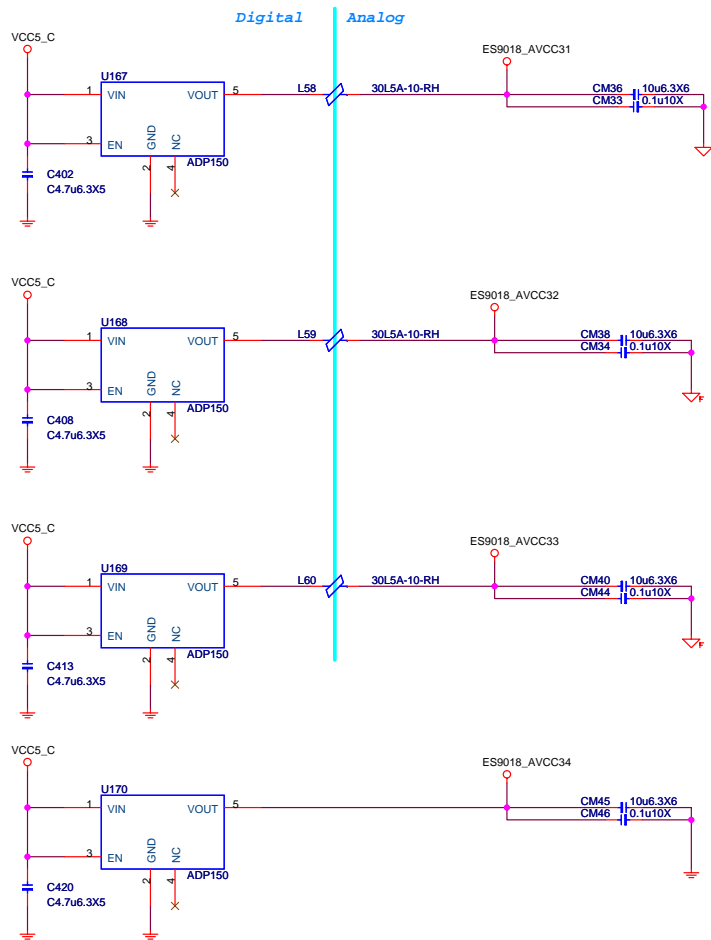
	Gain=1.5 Vrms=1.725
32 ohm	92.99mW

ESS9016 Vrms = 1.2V

	Gain=1.5 Vrms=1.8
32 ohm	101.25mW

$$3.3 * (6.34 / 16.34) = 1.28V$$

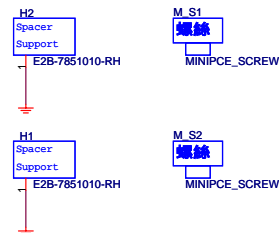
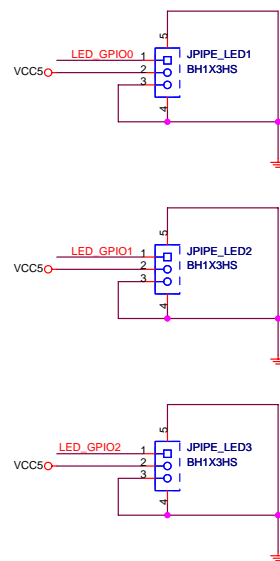
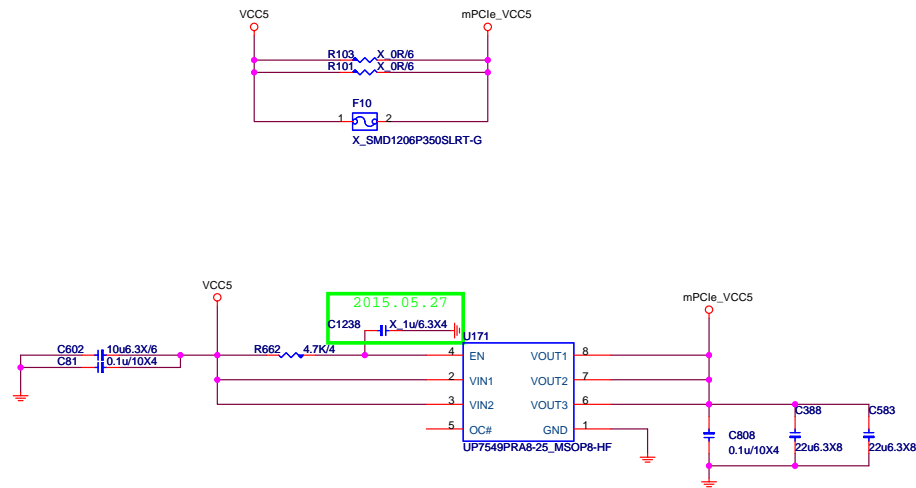
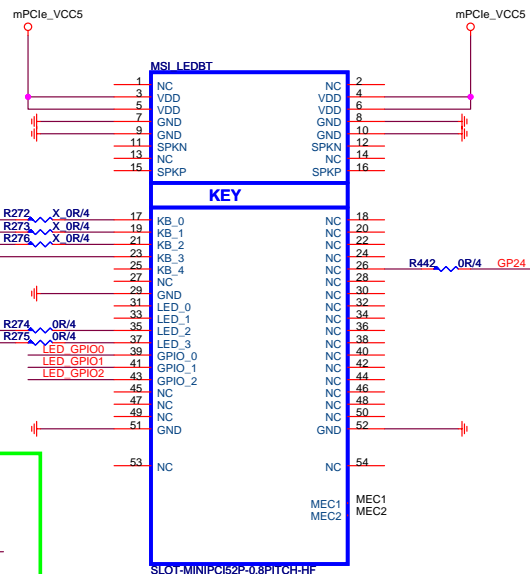




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E2400 Giga LAN

CHOKEL1:
L04-47A7690-M26,
AVL: L04-47A7870-C08

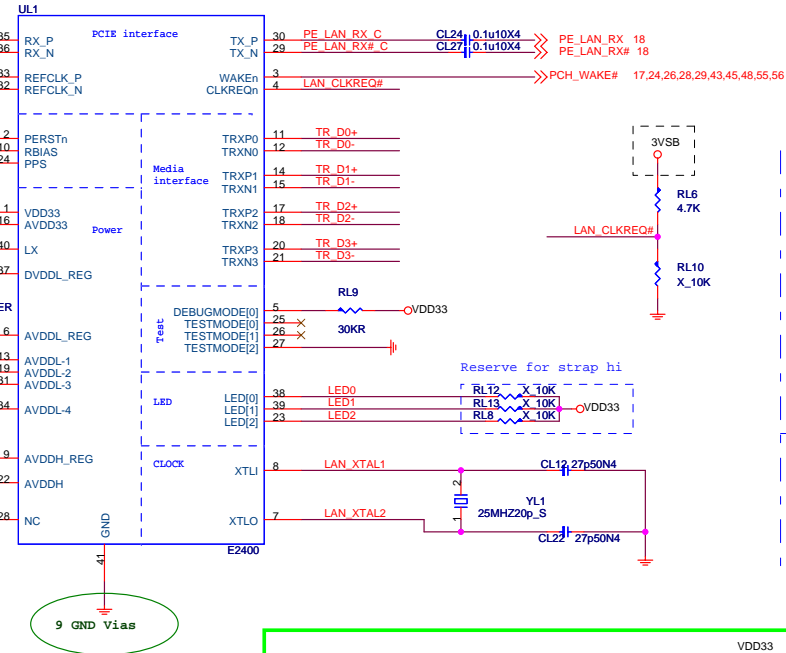
Close to pin40
close to CHOKEL1
(<200mil)

LL1:
L02-3018023-C08
L02-3018023-T19

22,23,30,38,43,69 ALL_LED_OFF#

Close to Pin37

place near pin <200mil



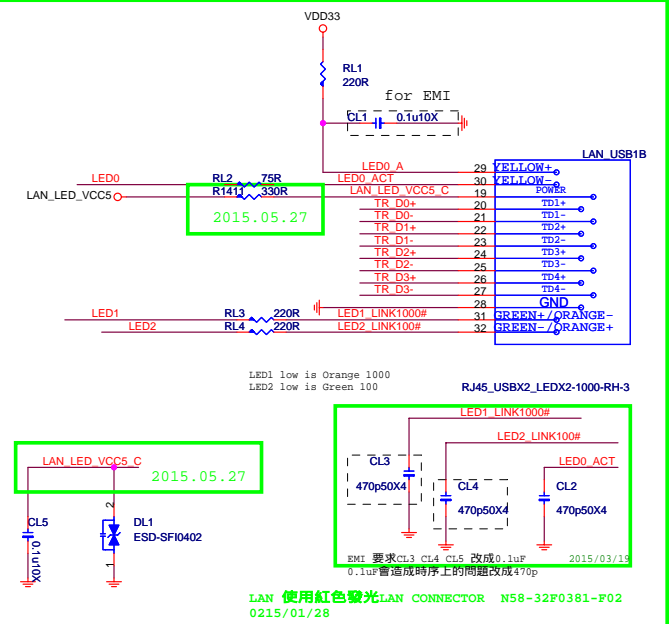
note:

LED0:
1=High core voltage
0=Low core voltage

LED1:
1=SWR mode
0=LDO mode

LED2:
1=25MHz clock
0=48MHz clock

VDD33 >= 30mils;
AVDD33 >= 30mils;
AVDDH >= 20mils;
AVDDL >= 20mils;
DVDDL >= 20mils.
Pin LX to L1 >= 30mils.

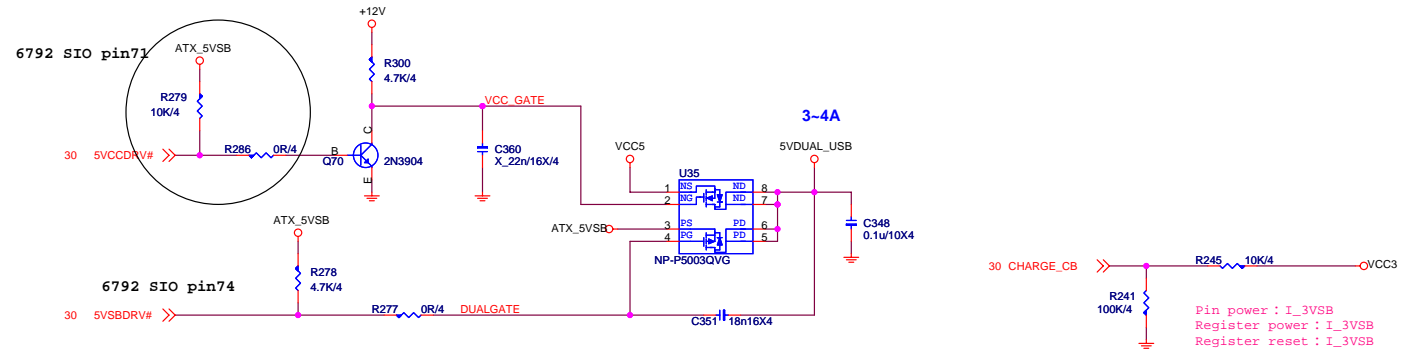


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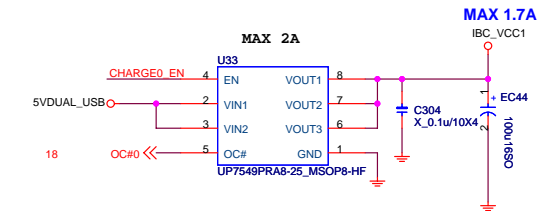
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Size	Document Description	Rev
Custom	LAN RTL8111G/8106E	1.1
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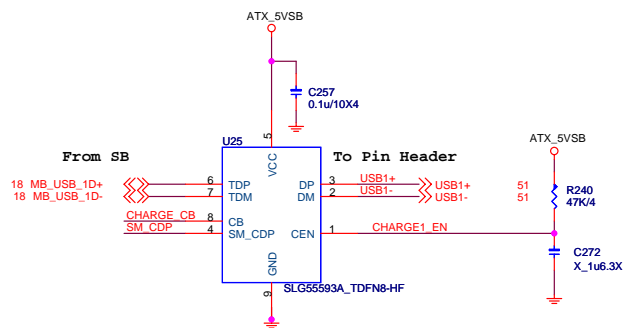
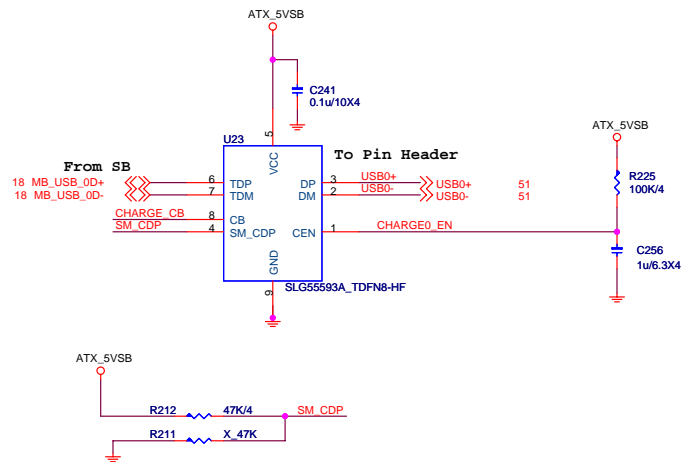
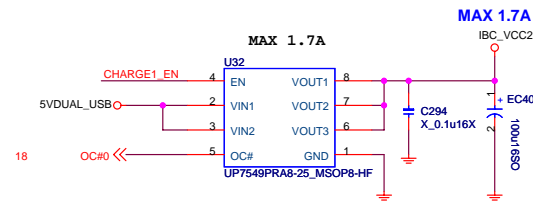
5VDUAL_USB

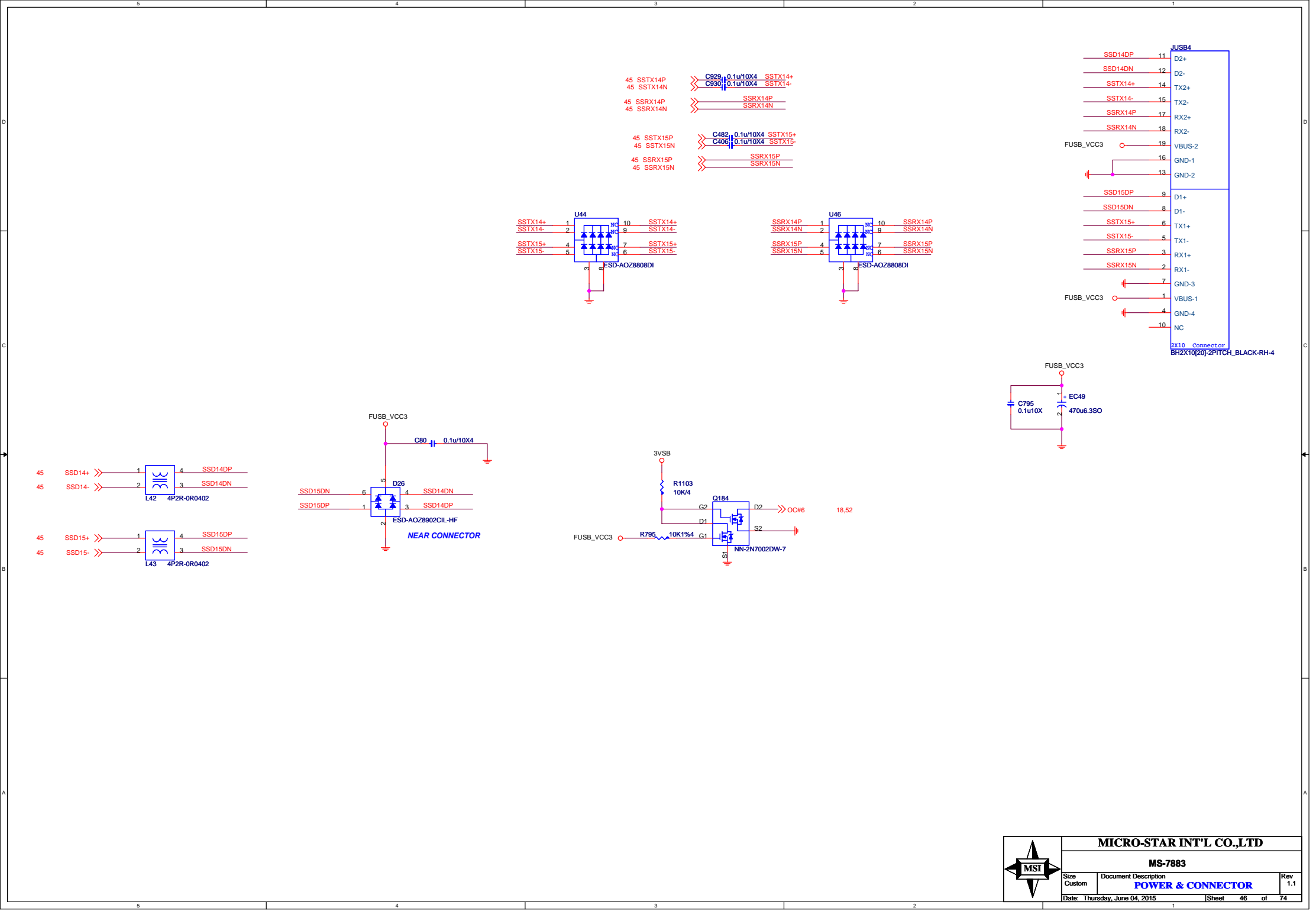


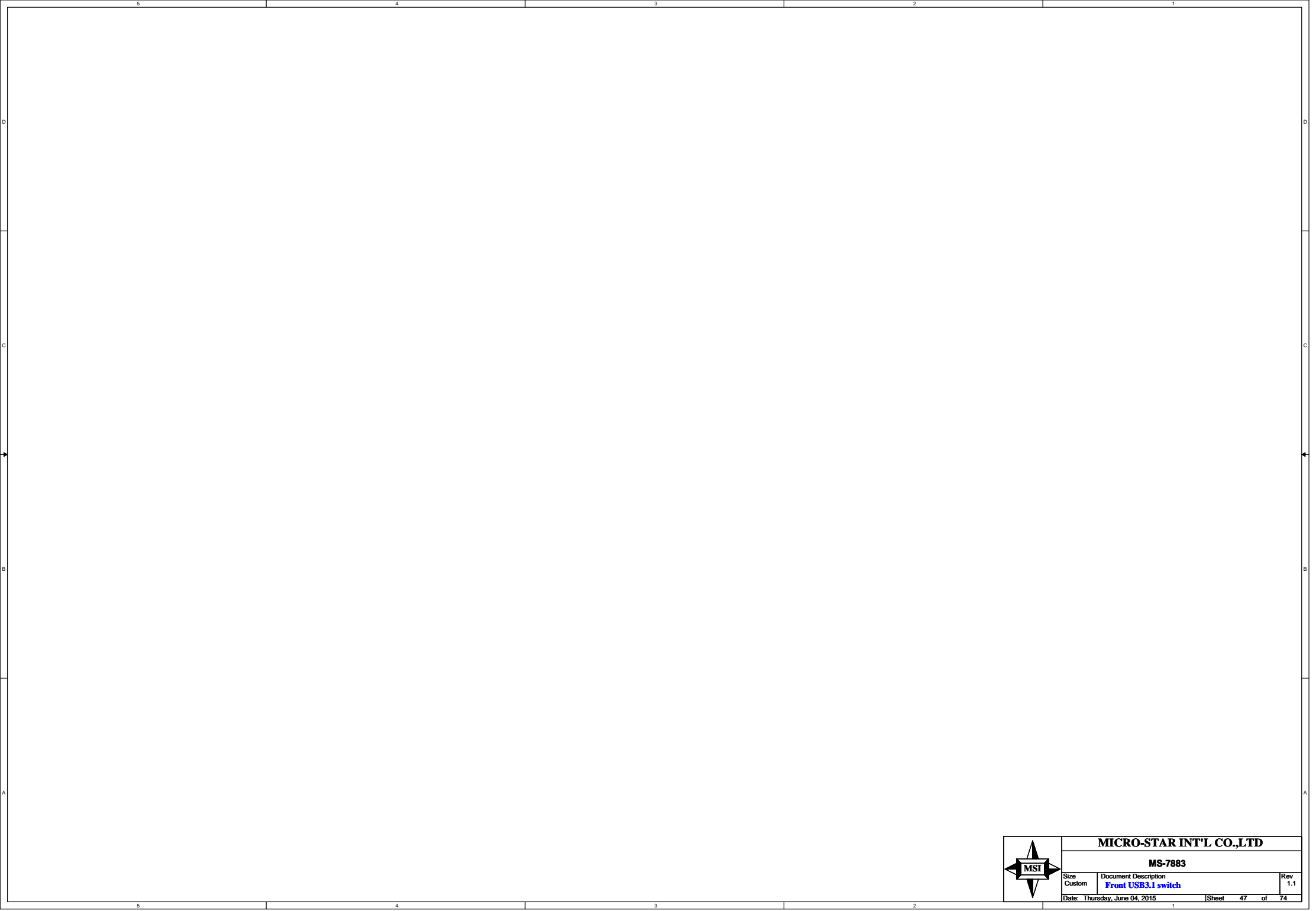
USB POWER PORT 0 For USB Charging



USB POWER PORT 1 For USB Charging





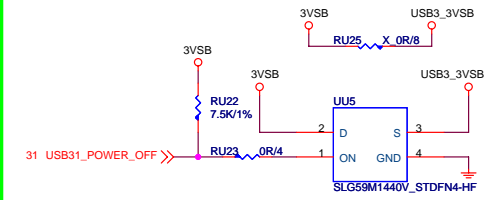


Minimun gap should be greater of
>15mil with other signal.

Power Consumption

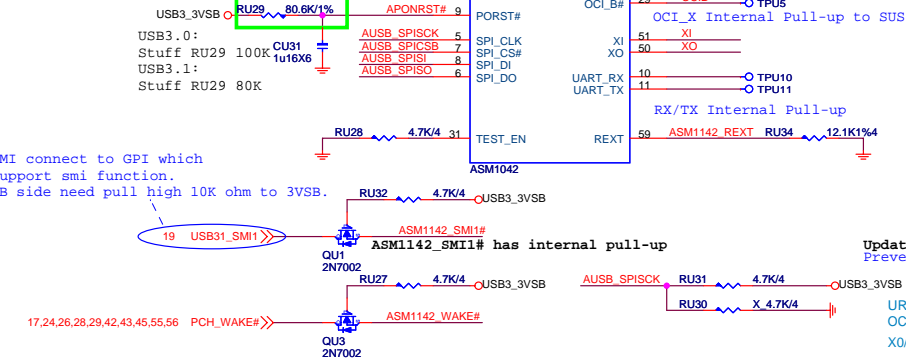
	3.3V	1.05V(1.2V)	3.3VSUS	1.05VSUS(1.2VSUS)	Total Power
ASM1042AE	95mA	300mA	65mA	9.5mA	852.975(mW)
ASM1142	245mA	634mA	1mA	1mA	1573.8(mW)

USB3.1 power switch



USB3.0:
Stuff RU40 & RU42
Unstuff RU39 & RU41
USB3.1:
Stuff RU39 & RU41
Unstuff RU40 & RU42

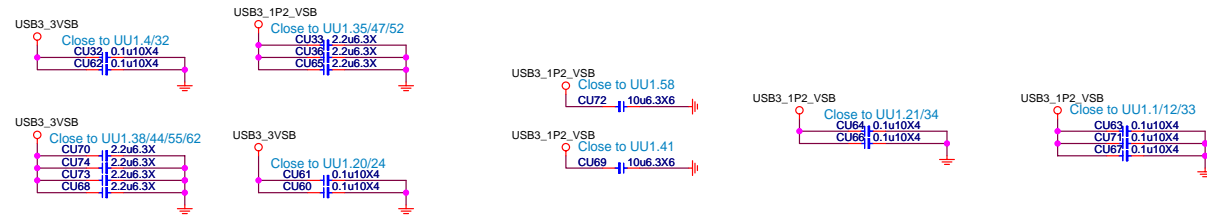
20150309 换成80.6K



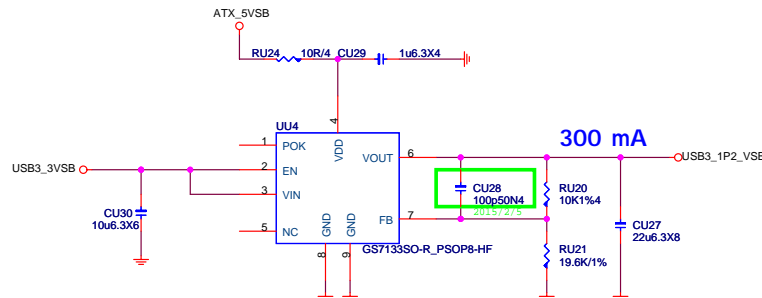
Update 2011.10.14
Prevention crystal not work yet.

UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8
X0/XI (95hm-Diff,Spacing 30mil)

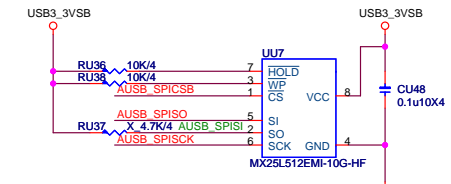
ASM1042 3VSB Circuit



ASM1042 1.2VSB Power



EEPROM

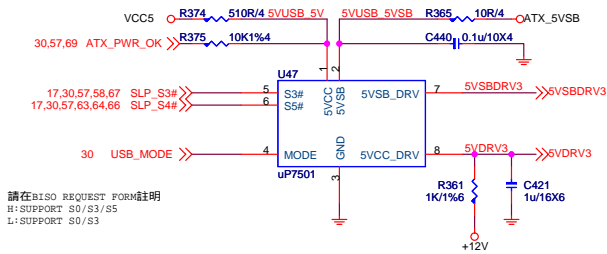


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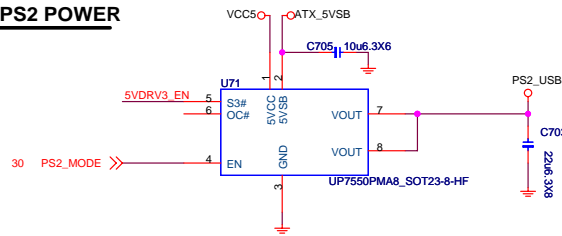
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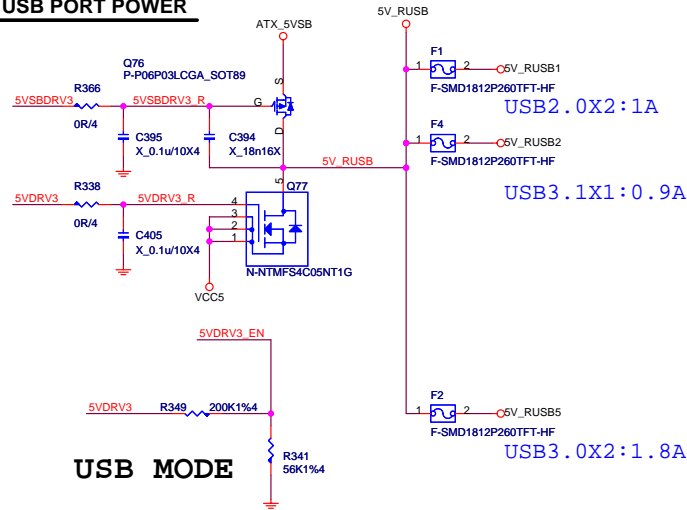
USB POWER



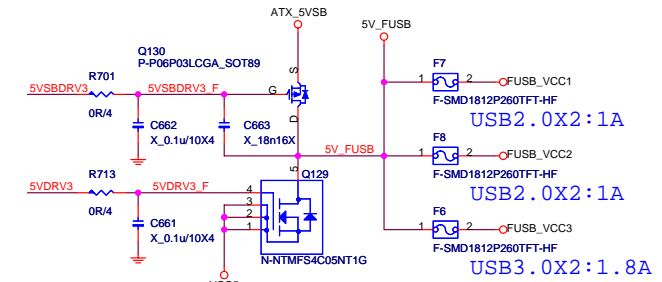
PS2 POWER



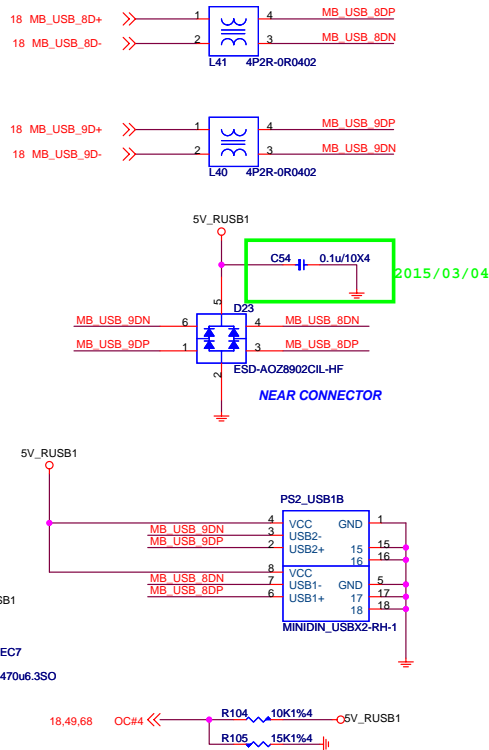
REAR USB PORT POWER



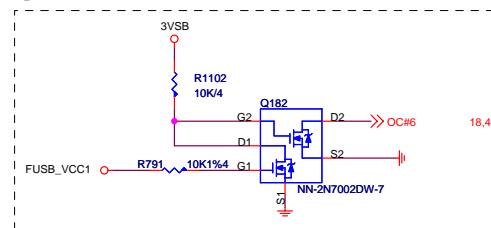
Front USB PORT POWER



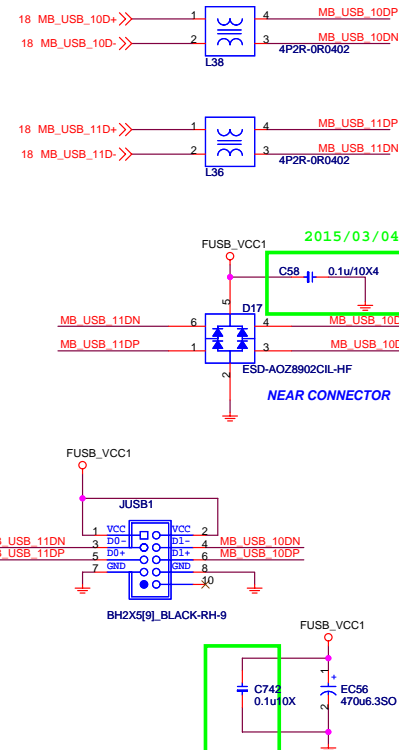
REAR USB PORT 8,9 (With PS2)



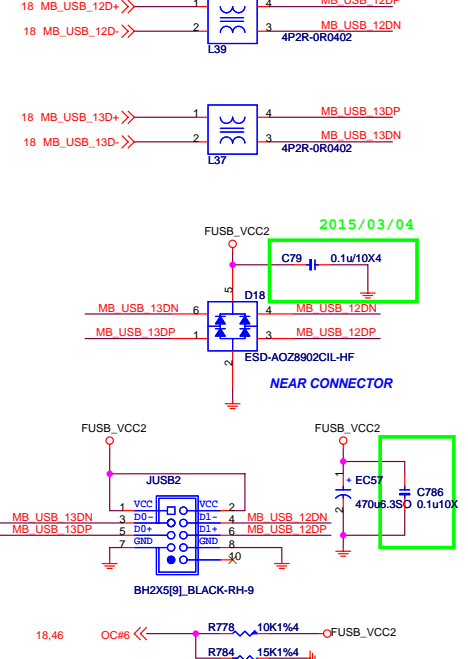
Modify 2014.12.18
From OC5 to OC6
Update 2014.12.30



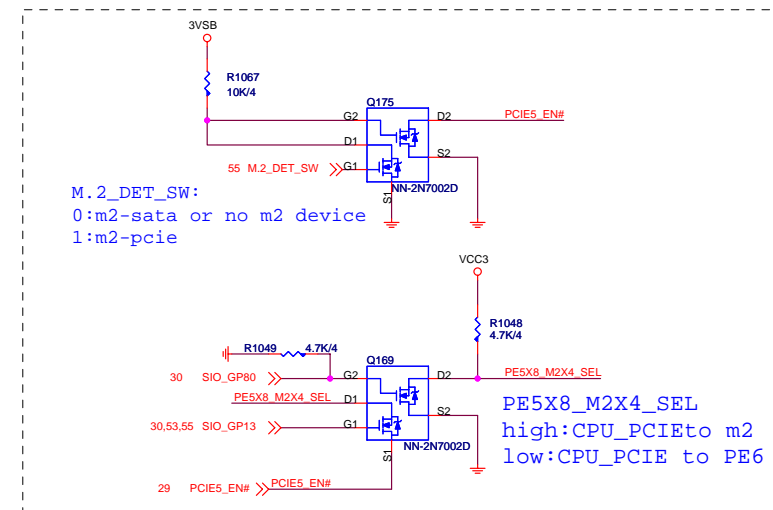
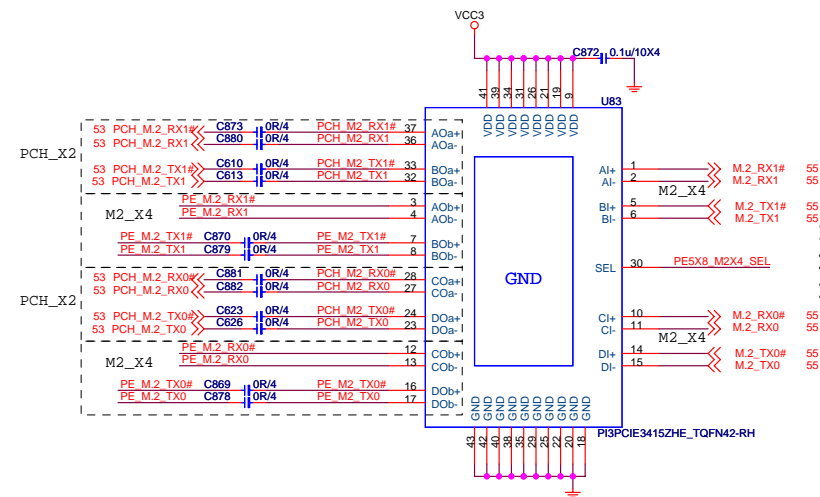
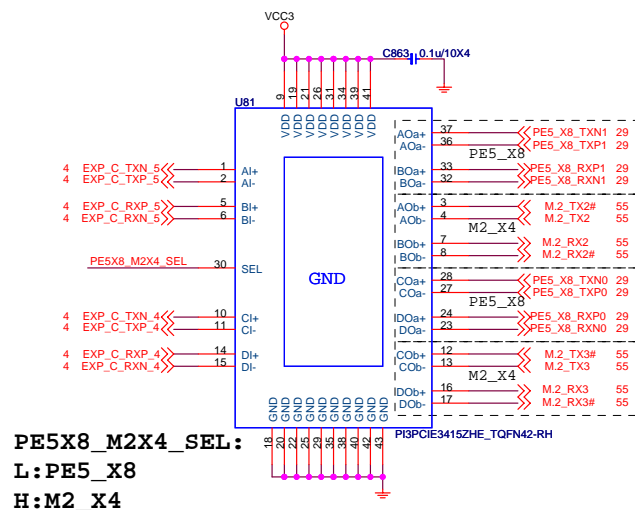
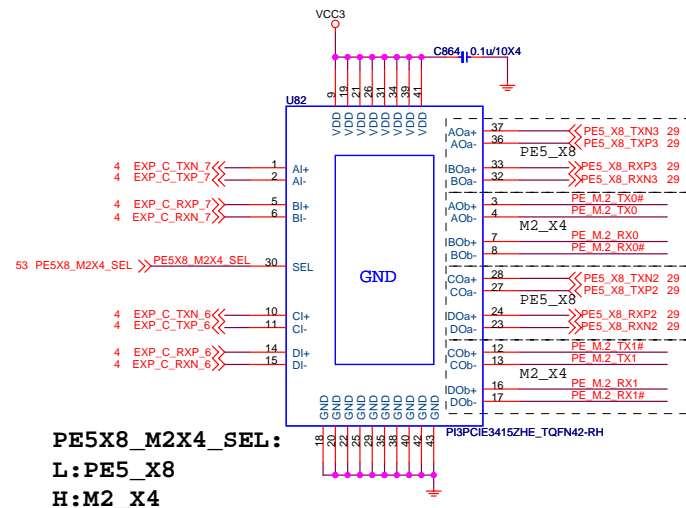
FRONT USB PORT 10,11



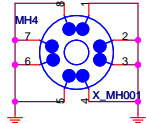
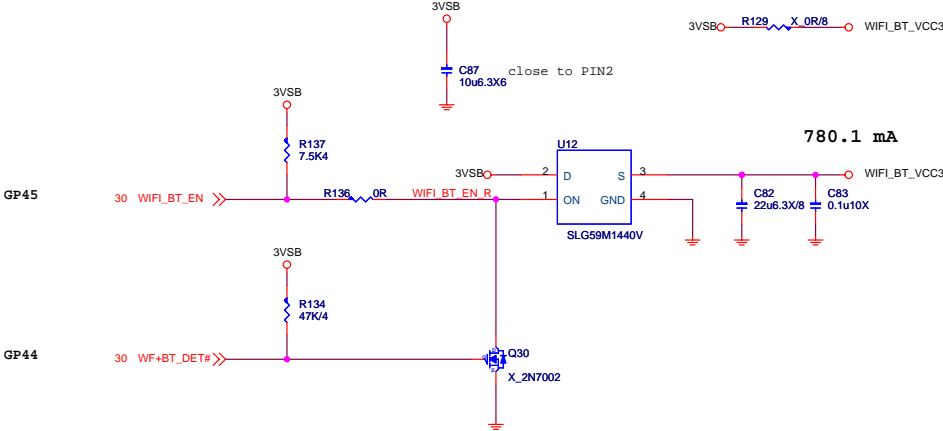
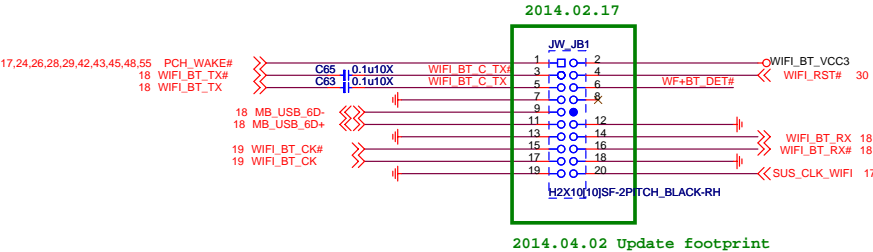
FRONT USB PORT 12,13



PCIE5 & M.2 Switch

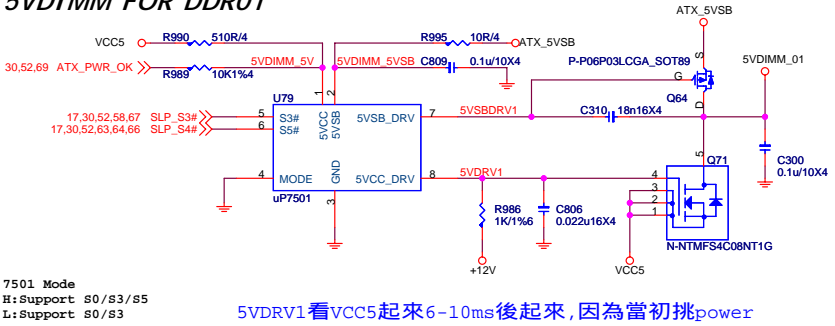


WIFI + Buletooth

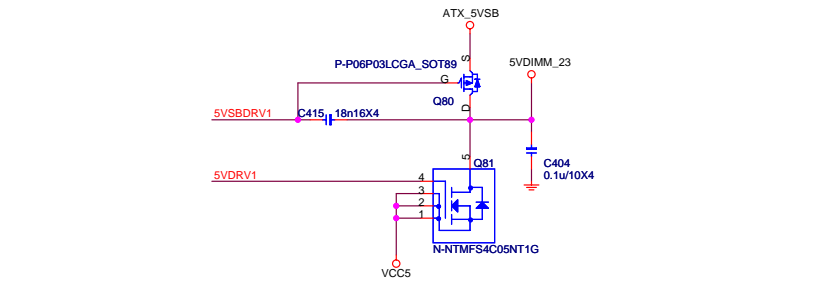


2014.04.02 Update footprint

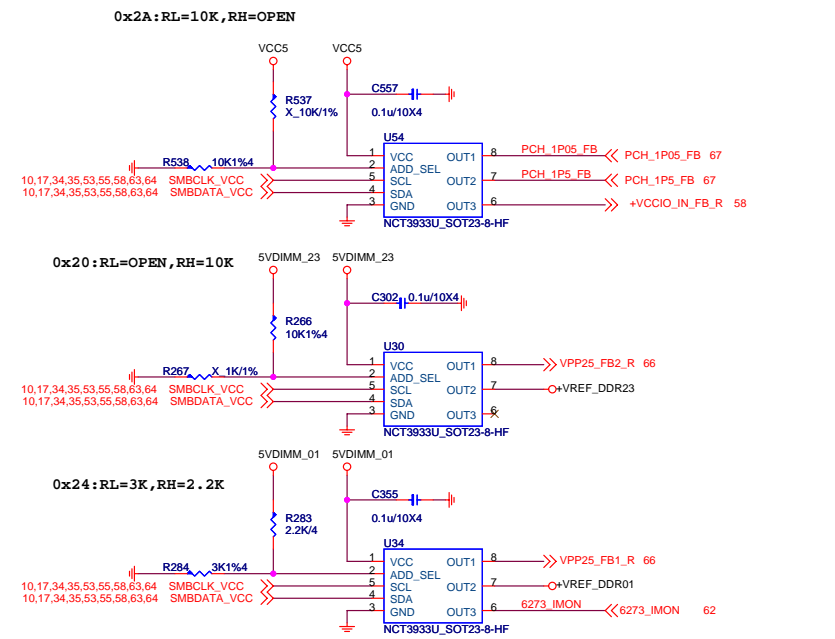
5VDIMM FOR DDR01



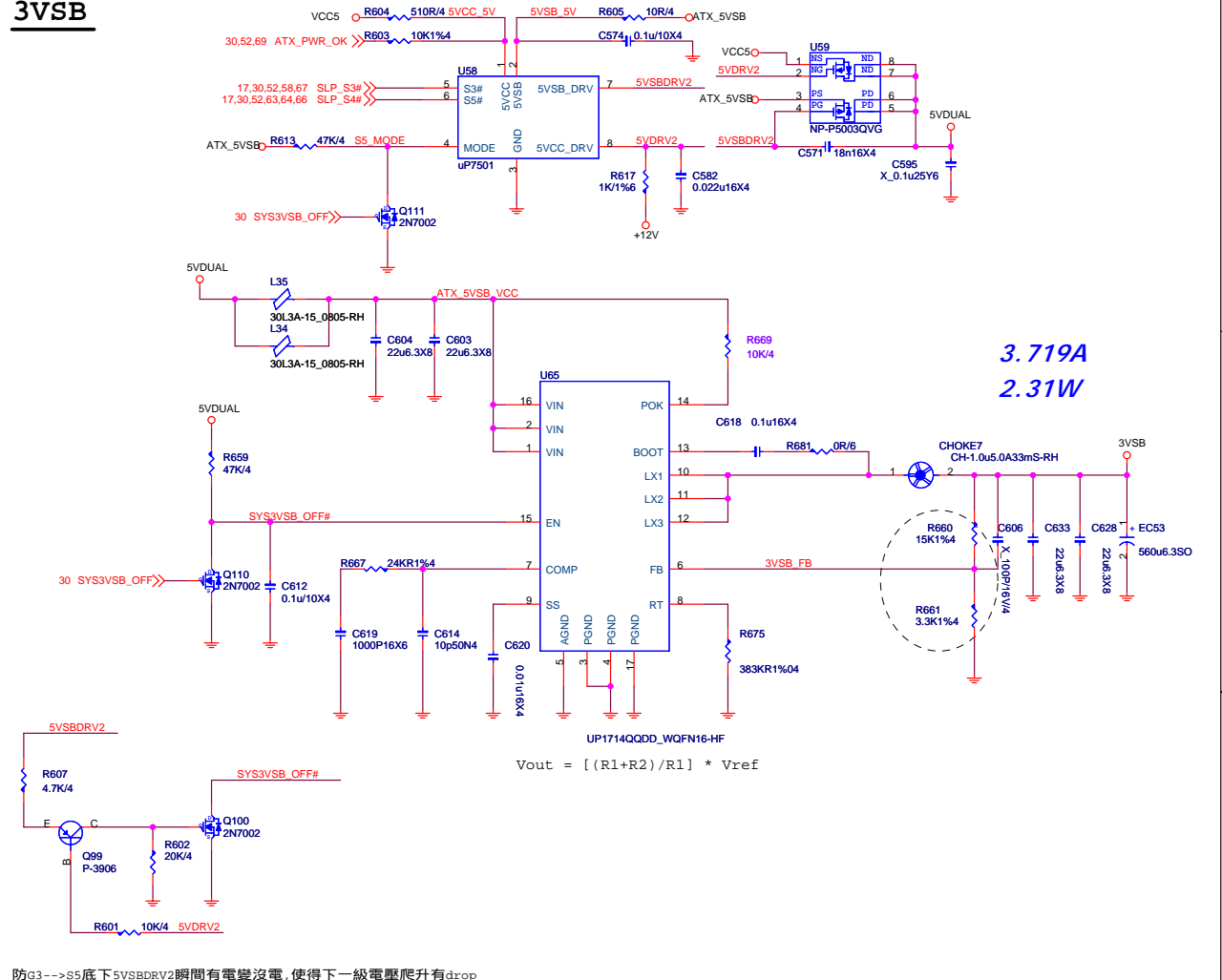
5VDIMM FOR DDR23



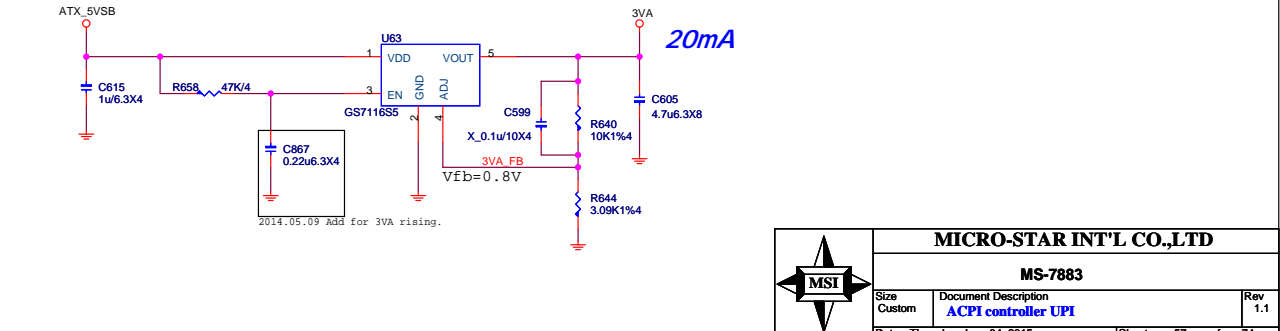
VOLTAGE CONSOLE

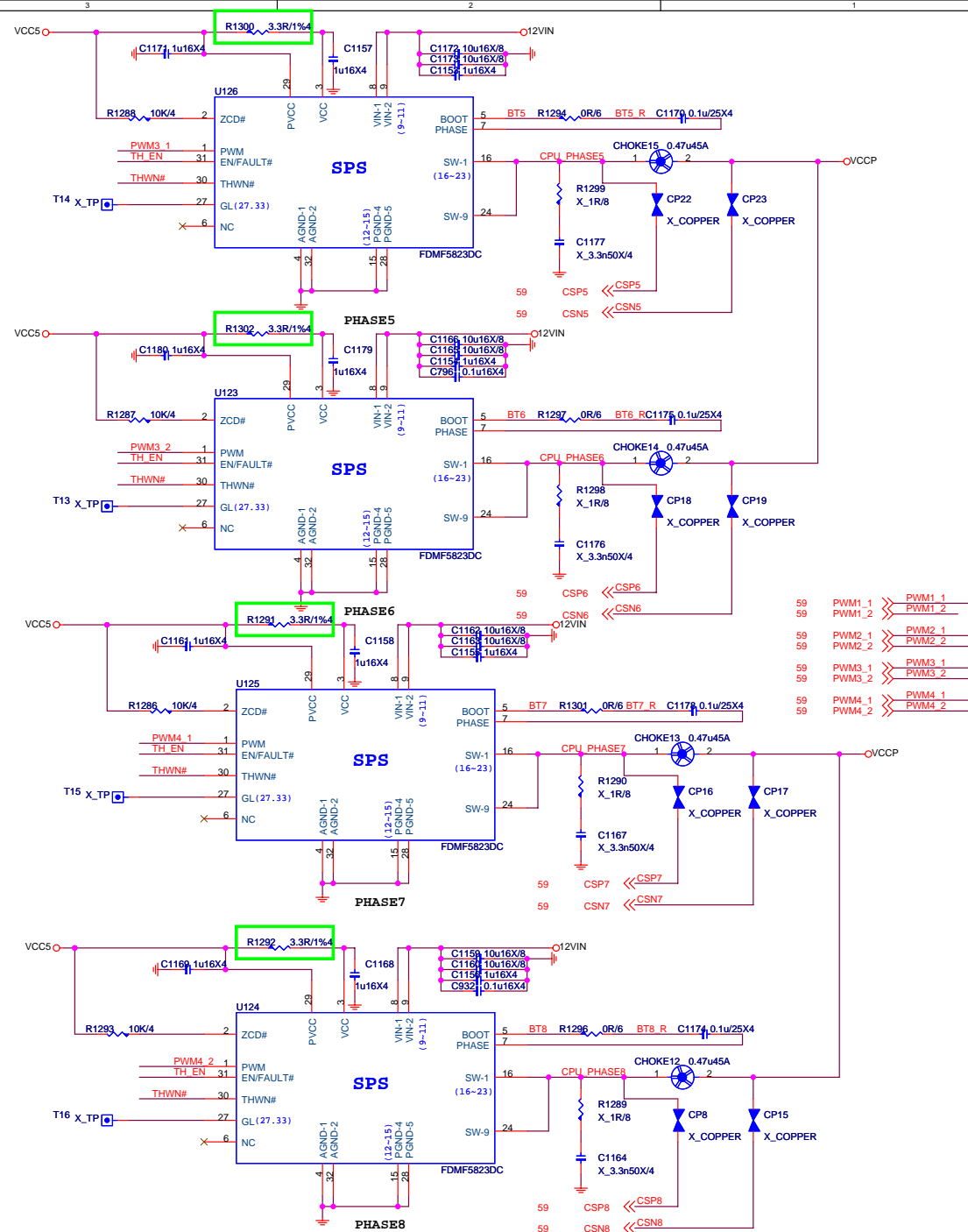
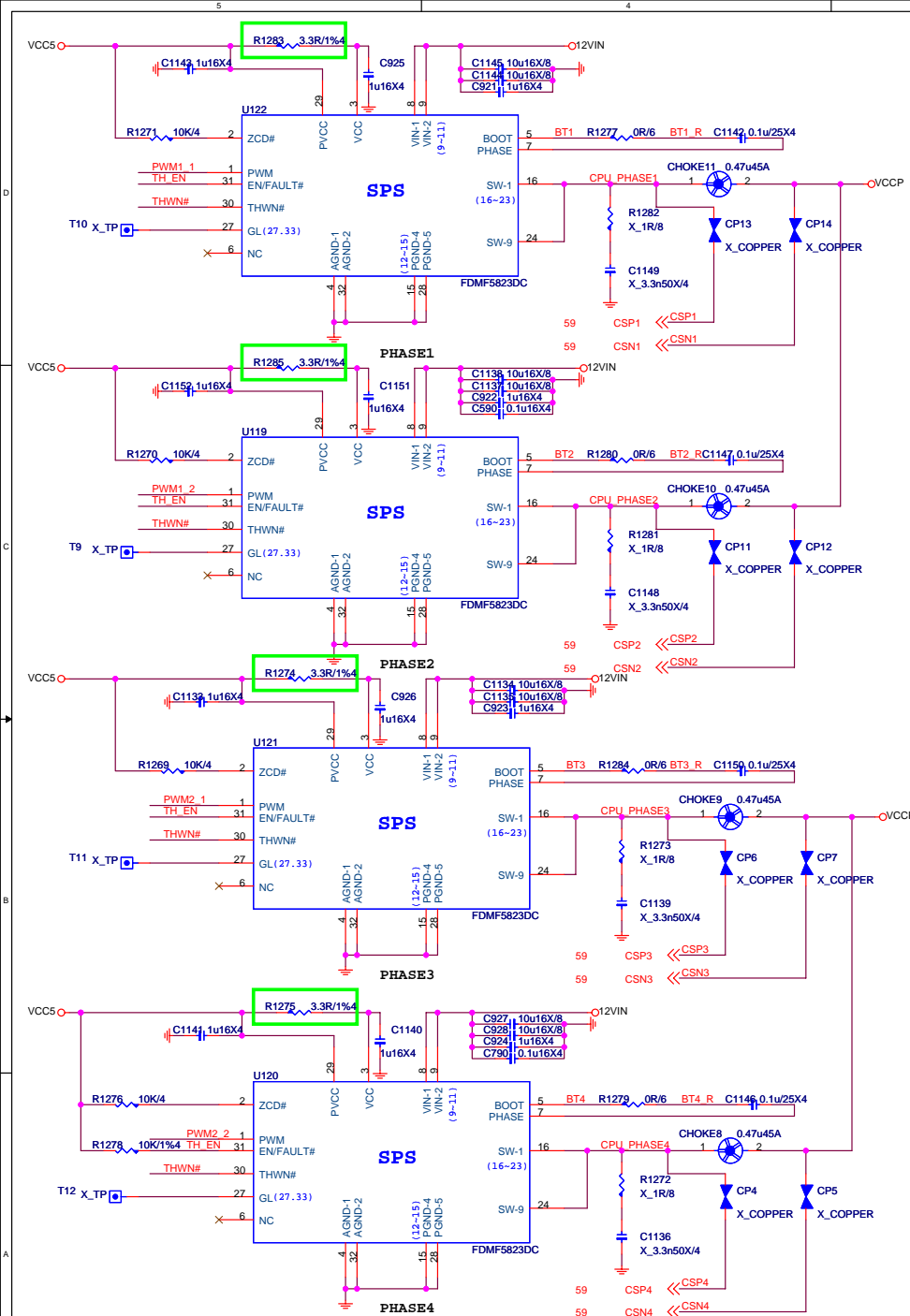


3VSB



3VA





61 TH_EN << TH_EN
3.61 THWN# << THWN#

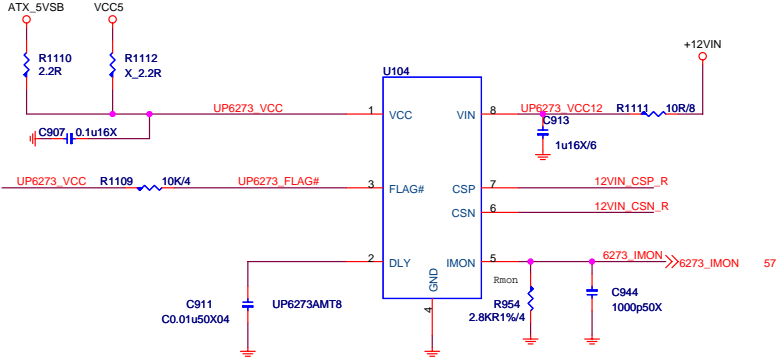
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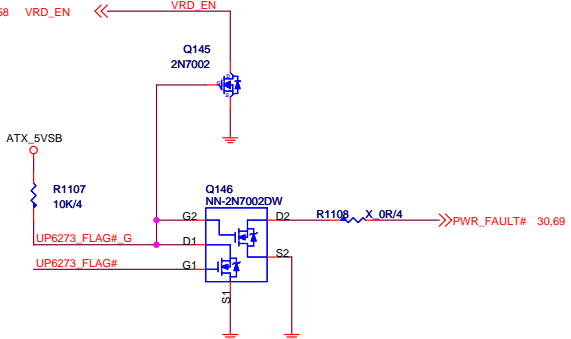
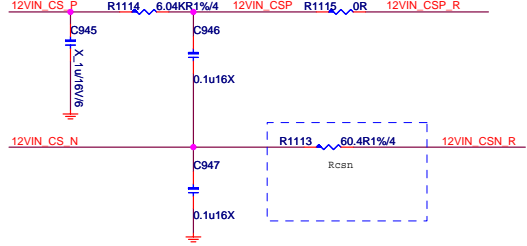
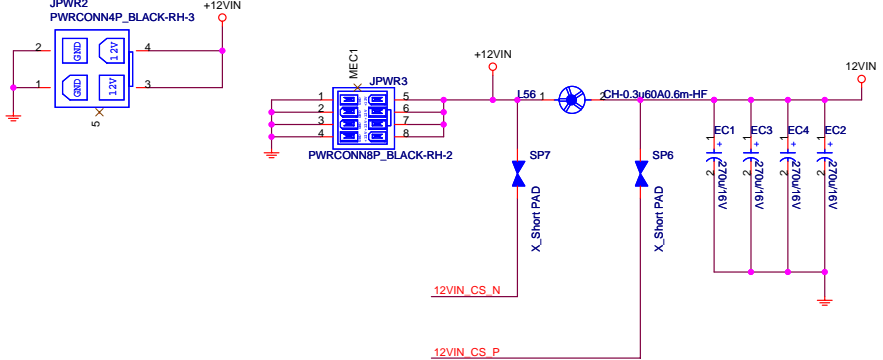
POWER METER
OCP: 120A



$$I_{in} = (V_{mon} \cdot R_{csn}) / (R_{mon} \cdot R_{dc})$$
$$V_{mon} = 1.2$$

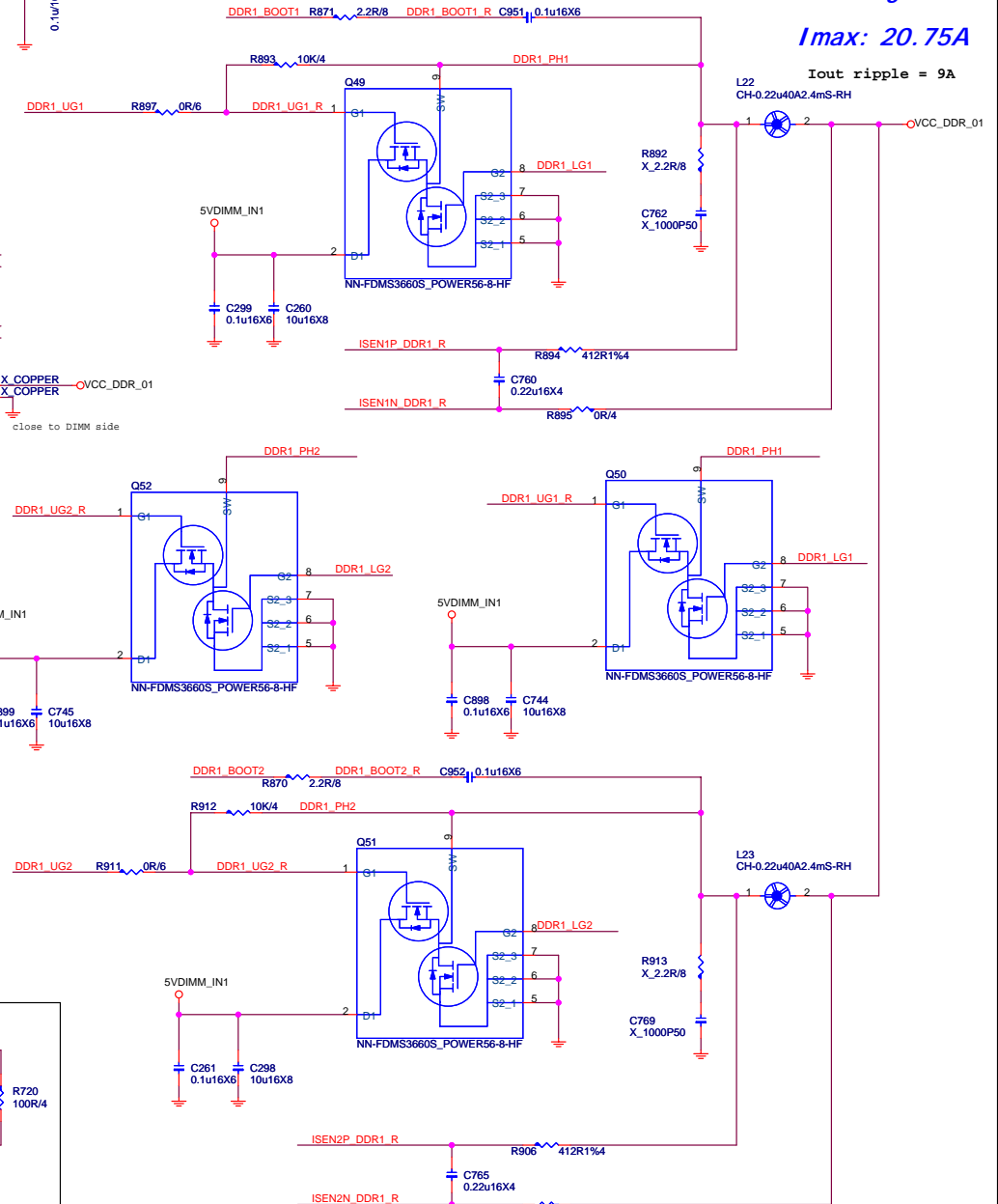
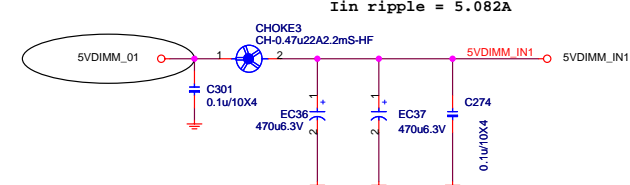
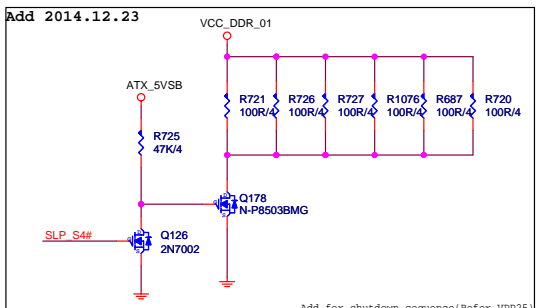
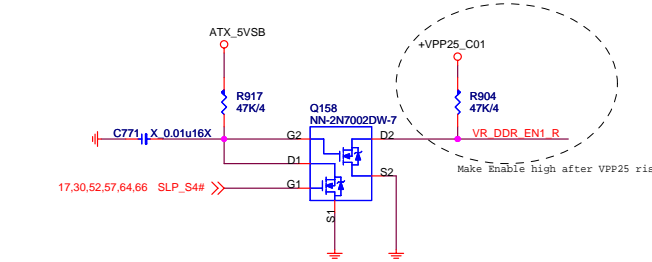
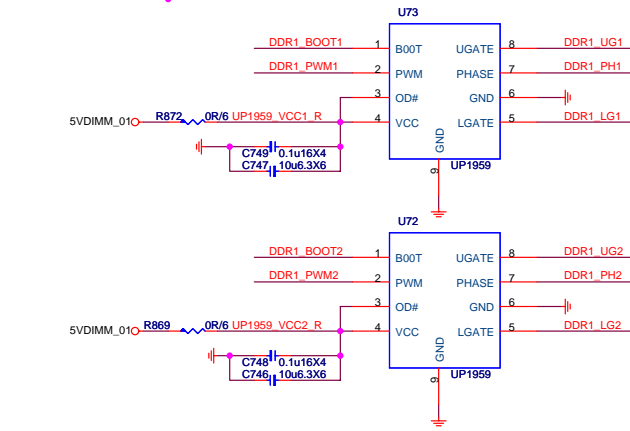
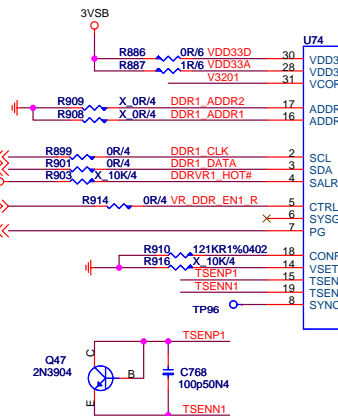
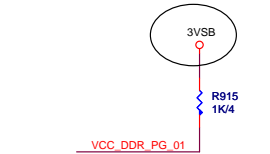
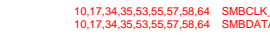
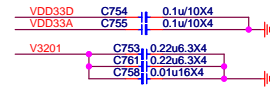
can change OCP trigger level by Rcsn and Rmon

$$(1.2 \cdot 0.2) / (10K \cdot 0.3m) = 80A$$



DDR Power1-FV3203-2-Phase

DDR4_1.2V 11A, OC margin=44A
OCP:66A for 2Phase



OCP=64A
OC margin=44A
I_{max}: 20.75A

I_{out} ripple = 9A

DDR Power1-PV3203-2-Phase

DDR4_1.2V 11A, OC margin=44A

OCP:66A for 2Phase

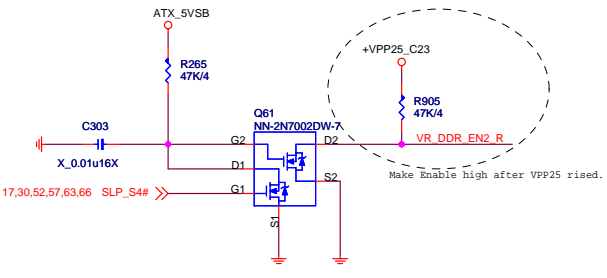
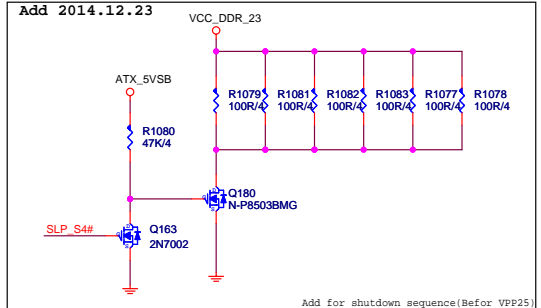
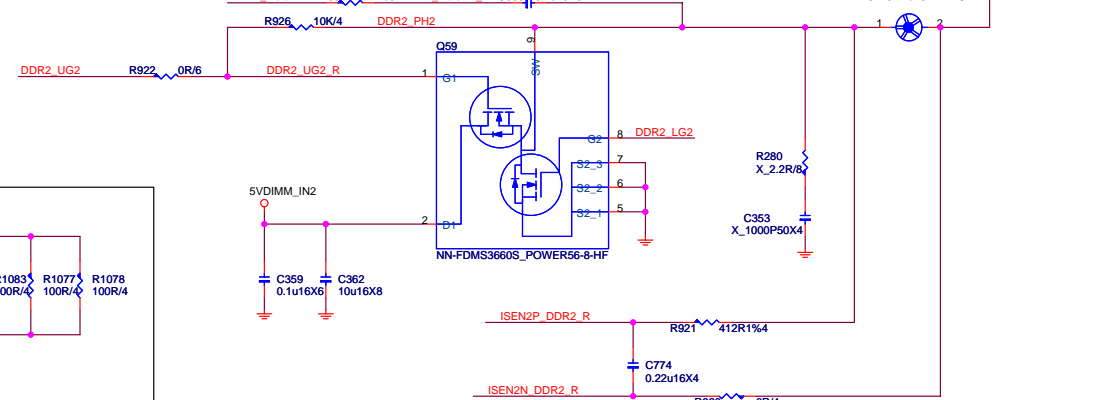
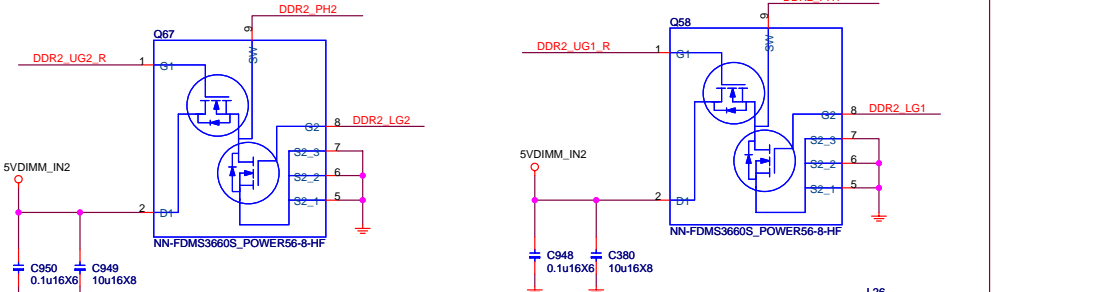
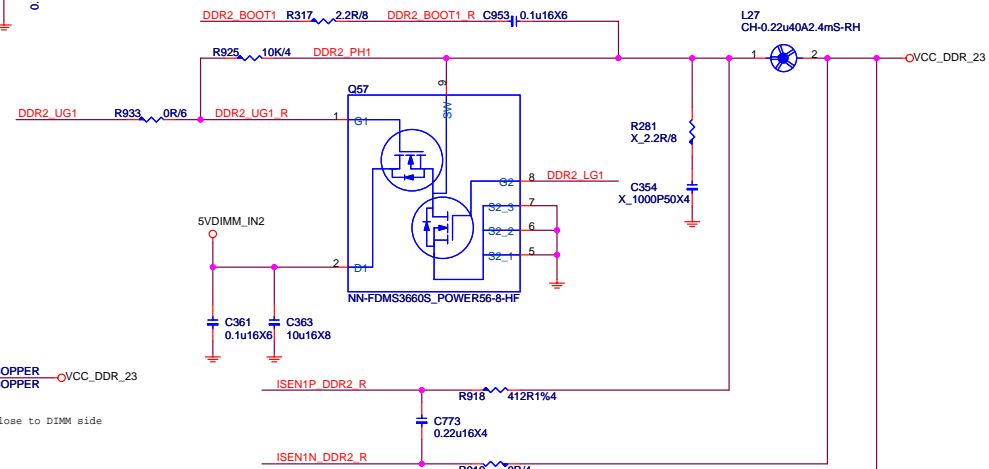
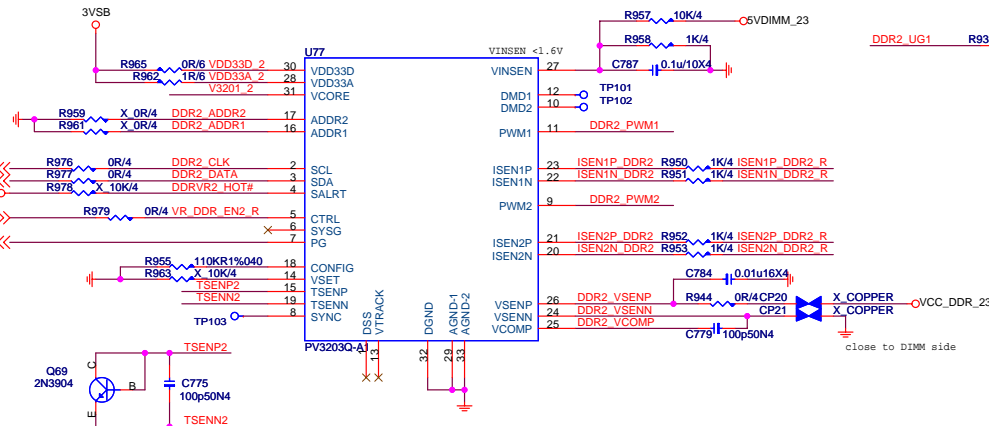
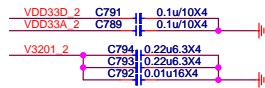
Iin ripple = 5.082A

OCP=64A

OC margin=44A

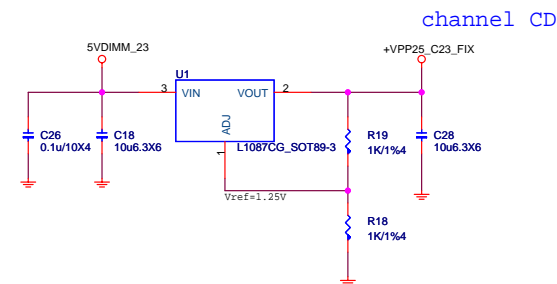
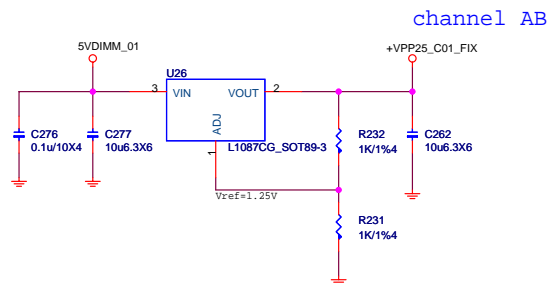
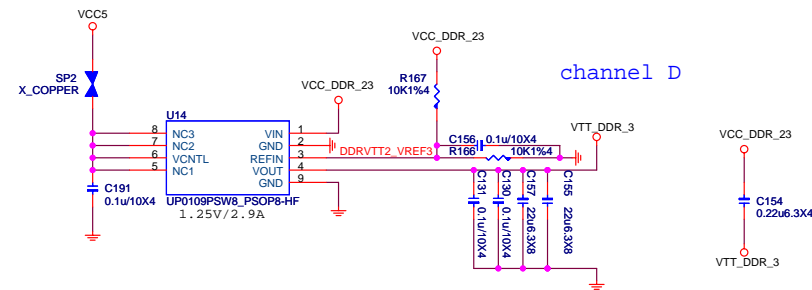
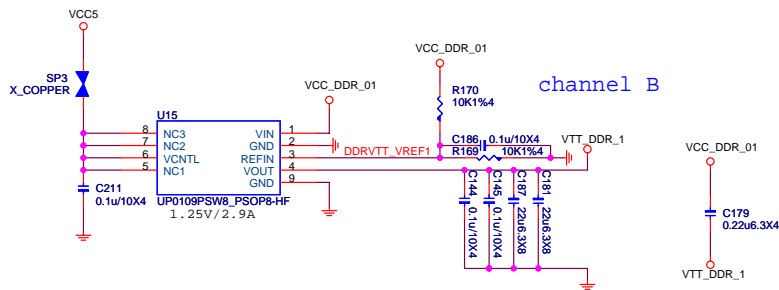
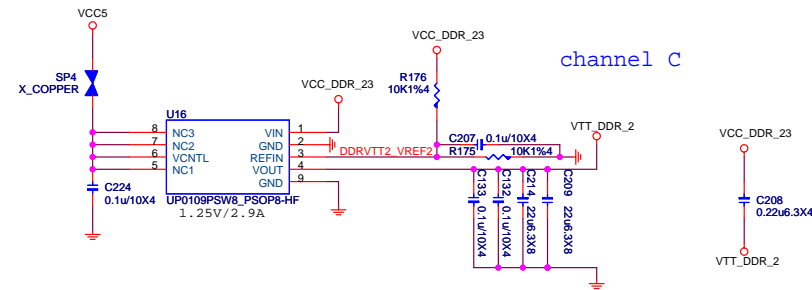
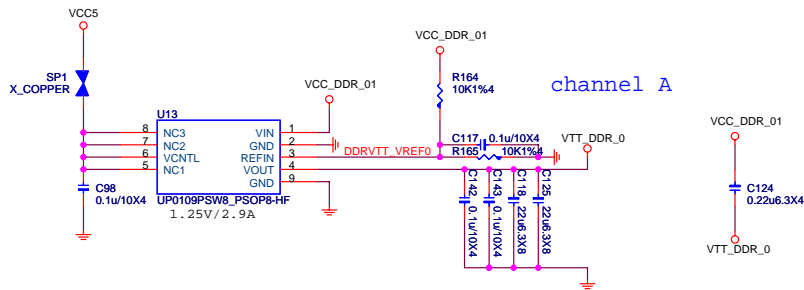
I_{max}: 20.75A

I_{out} ripple = 9A

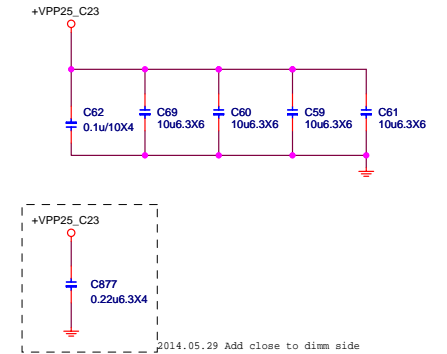
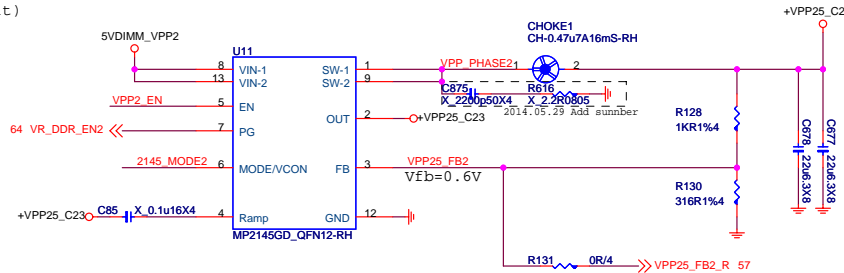
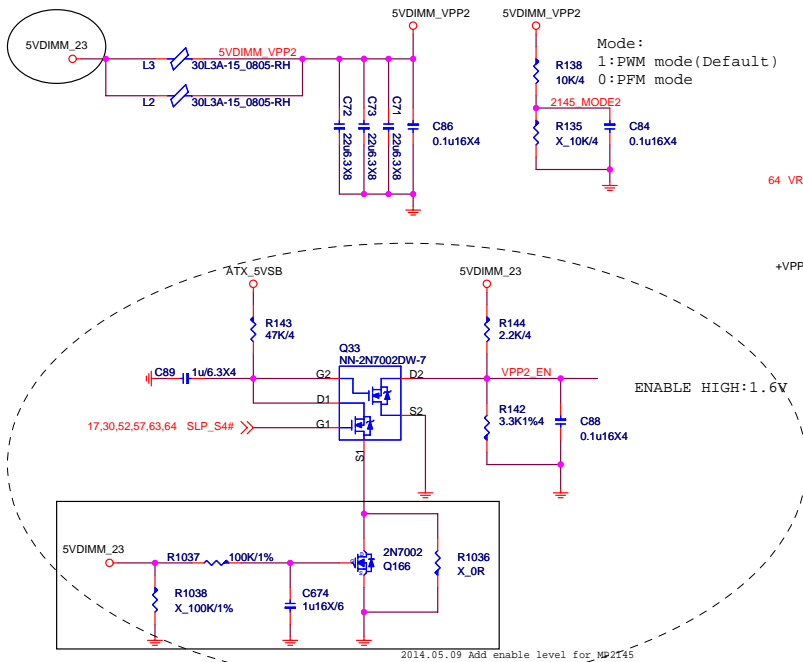
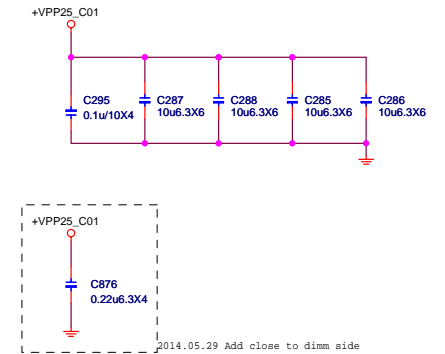
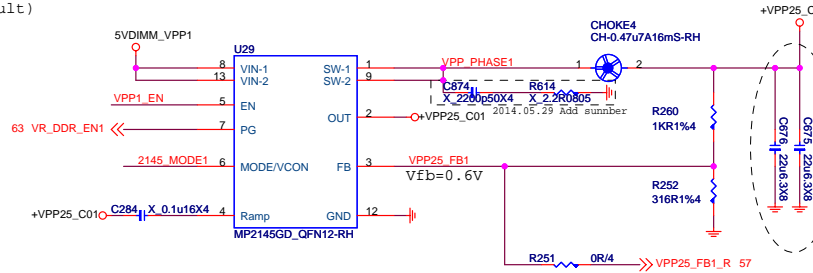
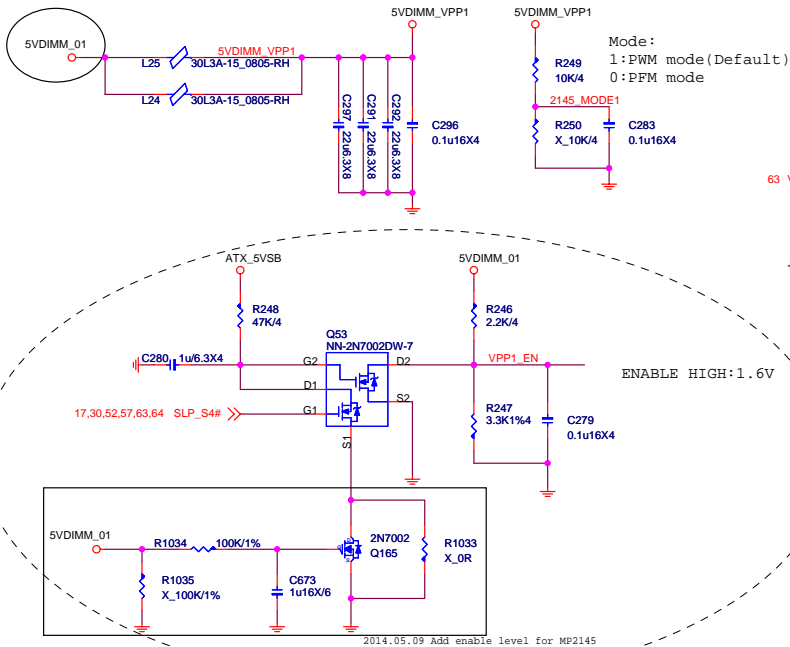


4DIMM :1.2A FOR DDR VTT

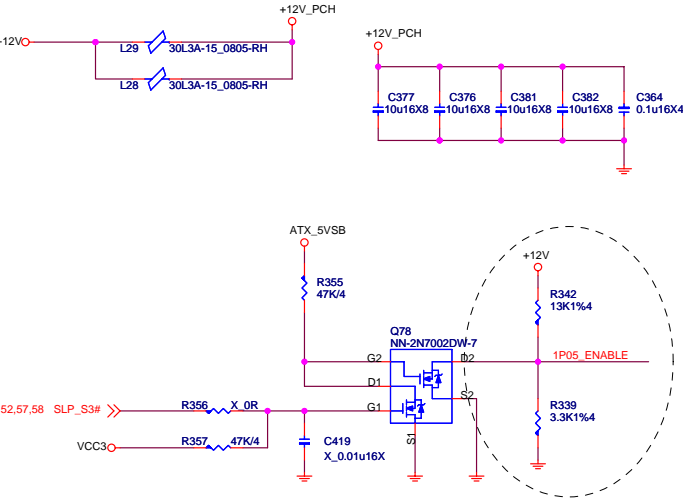
4DIMM :3A FOR OC margin



4DIMM :6A FOR DDR VPP

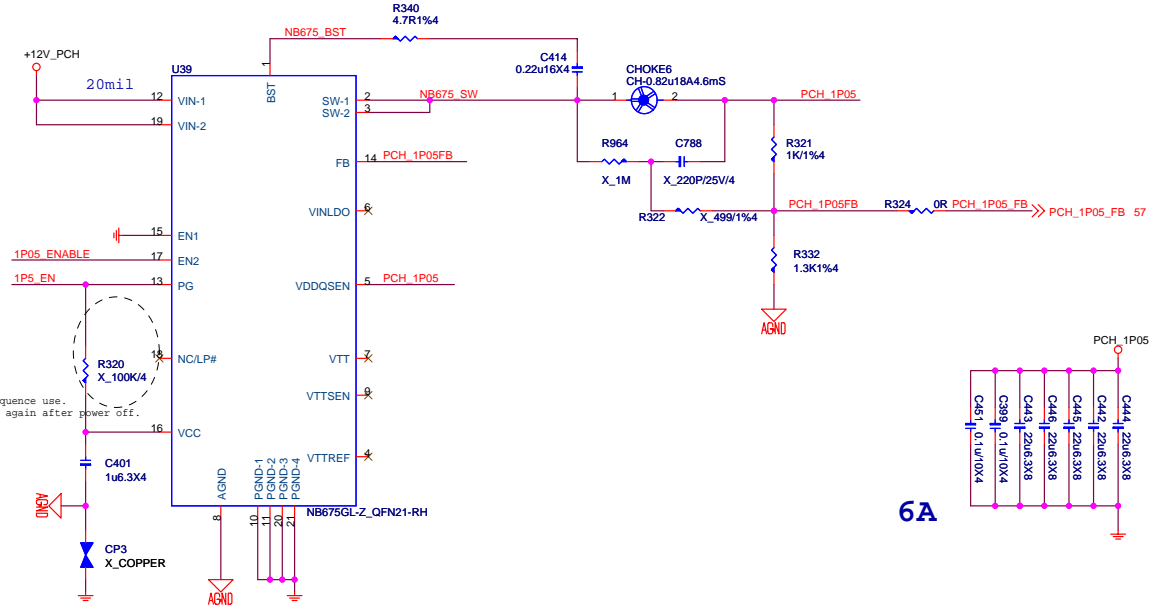


PCH Power:1.05V
PCH Core 6.504A



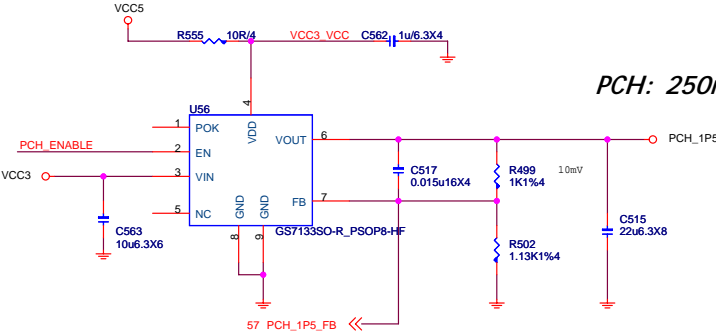
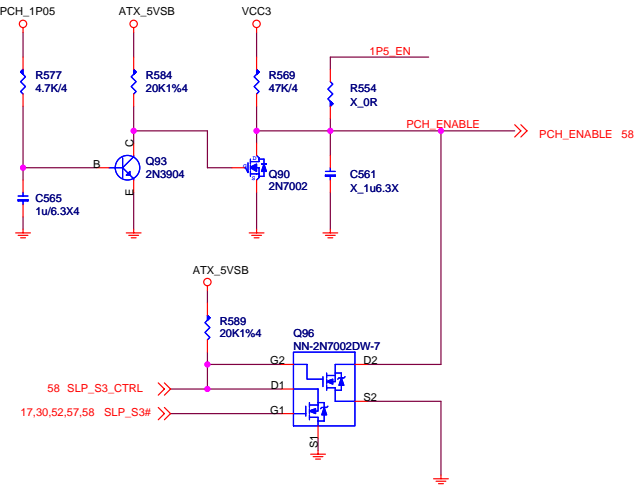
For internal power down sequence use.
Make sure Pin 13 no rising again after power Off.

MAX 10A
ILIMIT=10A~12A 峰谷

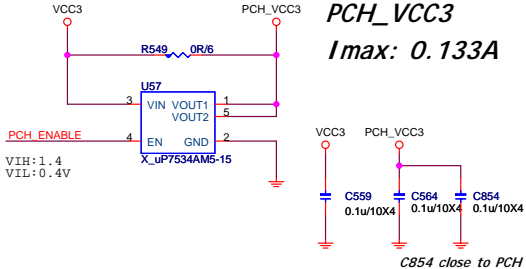


6A

Waiting PCH_1P05 Ready



PCH: 250mA

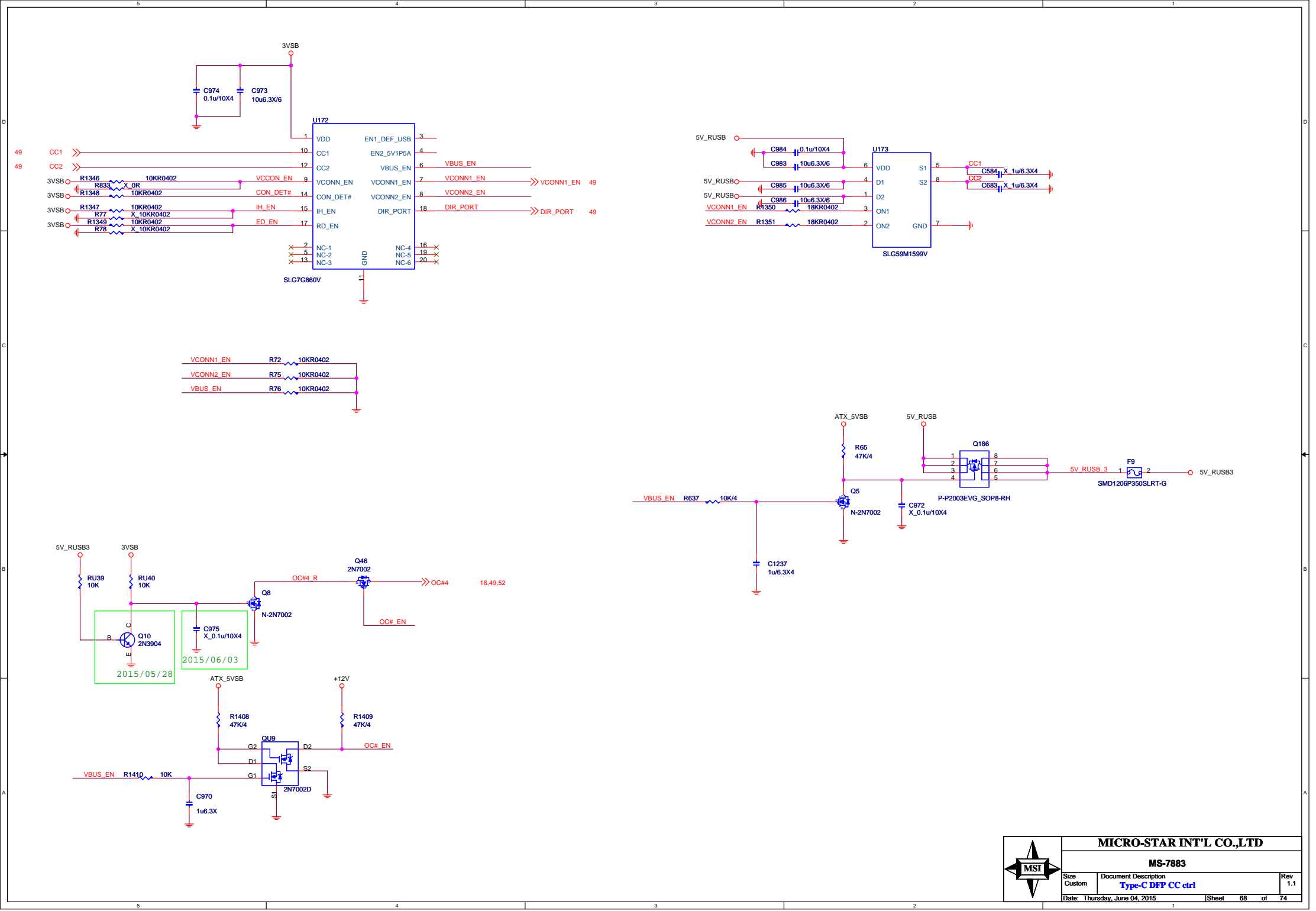


PCH_VCC3
Imax: 0.133A

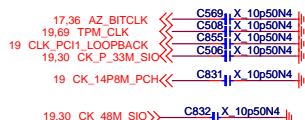
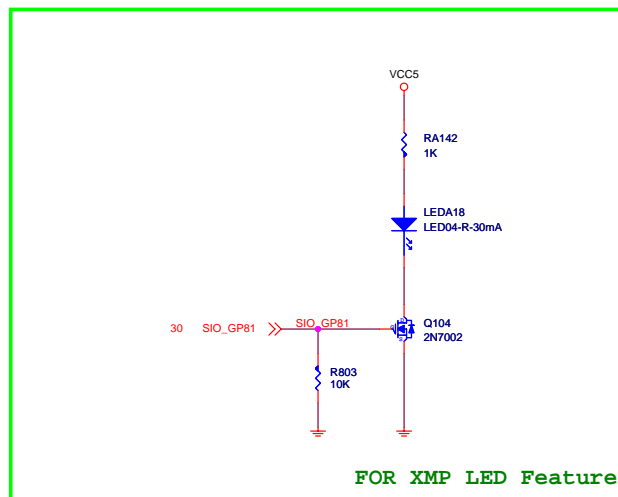
C854 close to PCH



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Reserve debug port 5020

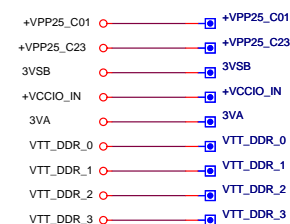
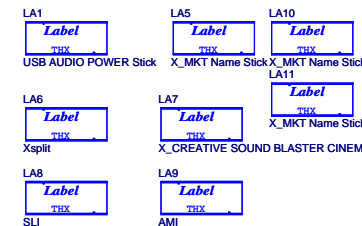
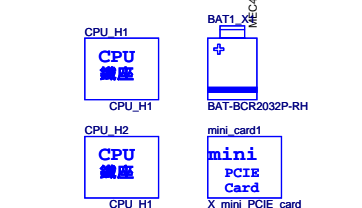
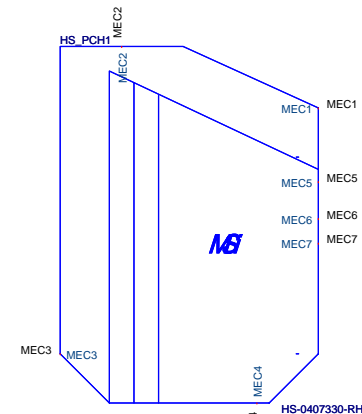


7 CPU_DEBUG_EN_N << CPU_DEBUG_EN_N R942 976R1%4
3 CPU_TDO << CPU_TDO R940 75R/4

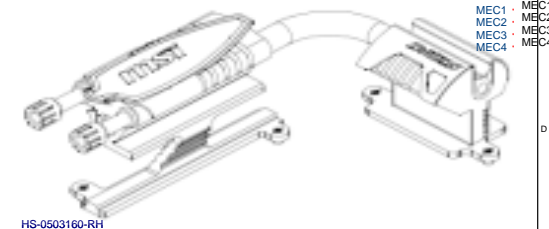
WITHIN 250MILS OF XDP CONNECTOR PIN



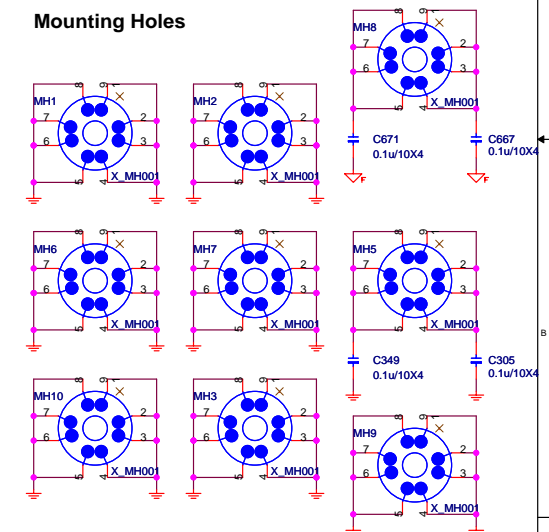
USB3.1	RU31-RST
ASM 1142	80.6K
X_ASM1142	X_80.6K1%0402
USB3.1-CONN	RU31-V
ASM 1142	19.6K
X_USB3.1-CONNECTOR	X_19.6K/1%



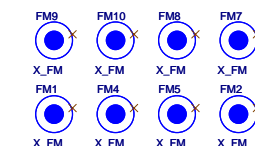
HS_MOS1



Mounting Holes



Optical Fiducial Marks-120



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